Electronics Packaging and Assembly Research and Development


The quality and reliability of electronic systems depend on the integrity of interfacial adhesion. Adhesion is critical at all electronics assembly levels. Material layers on a chip, package and system need to have excellent adhesion to each other.

Thin films are an integral part of chip devices and also are necessary at other levels of electronic systems. The quality and reliability of their interfacial adhesion defines the quality and reliability of the finished product. To assure interfacial adhesion integrity, numerous measurement techniques are employed. Most of these measurement techniques require the use of sophisticated and expensive equipment. Of the simpler techniques, one is tape peel testing which is usually used as a no-no-go screening test. This paper outlines its application as a valid quantifiable evaluation tool. In this narrative, testing, setup and measurement procedure is outlined for tape peel testing. The procedure was used successfully to evaluate and choose pretreatments to enhance interfacial adhesion of sputtered thin layers of various metals.

It is shown that the procedure provided results which could be validated through subsequent thick film peel testing.

Thin films are used industry wide in applications other than electronic systems; therefore, this study is applicable industry wide providing a quantifiable method to measure thin film adhesion.


Conventional printed circuit boards (PCBs) may be replaced by thinner metal-core boards for some applications, as well as for package substrates. Using thin, metal-core technology may provide advantages for radio frequency (RF) circuits and packages, and increase heat dissipation for high power applications.

The metal-core technology discussed in this paper has several layers including the metal core; electro coated dielectric, sputtered metal layers, and electroplated copper. For PCB and substrate reliability, it is important to have sufficient adhesion between the dielectric layer and plated copper. Sputtered metal layers with cleaning pre-treatments are one of the methods to improve the interfacial adhesion.

This paper describes an efficient testing method for the adhesion of a thin sputtered metal layer to a dielectric substrate. In this method, adhesive tape was attached to the surface and peeled off at 90 degrees in a tensile tester. Due to the sub-micron thickness of the sputtered layers, conventional peel test methods could not be applied. Typical adhesion testing of upper layers like paint coatings use a lattice pattern. The new method provided a convenient, repeatable way to evaluate the adhesion of three different sputtered metals with fifteen different pretreatment combinations. The test results were used to choose the sputtered metal and were later confirmed by testing the copper plated assembly using the metal adhesion specification in the industry standard IPC-TM-650.

A review of other methods and the need to identify an easy to use method which can provide
repeatable quantitative measurements.


As proliferation of handheld devices drives 3D packaging to achieve densification, embedding increased functionality into a chip is a natural complementary advancement in miniaturization. Ever increasing complexity of microelectronic design and functionality leads to the use of multiple surfaces for circuit development on wafers or individual die. Through-silicon vias, stacked die and stacked wafers, along with circuitry deposited on multiple surfaces and irregular shaped structures are some examples of 3D packaging. Laser patterning and via drilling on sapphire wafers and die with a 532 nm green laser has shown significant capabilities to make micro-features on and in the sapphire. Current structures include vias for die and wafer level interconnects, and patterned grooves for circuitry and antenna patterns. Other possibilities include pocket or trench patterning for adding passive components to the back of die or wafers. Backside patterning may be used for nano-imprinting of inks and other liquids. These grooves may also be used as micro-mixing or dispensing channels for use with nano-materials or liquids. All of these techniques may be applied to 3D die or wafer assembly and packaging.


Substrates play a critical role in the quality and reliability of electronic packages and systems. Metal core substrates provide opportunities with respect to strength, heat dissipation, and speed over common organic substrates. The metal core provides an opportunity for grounding enhancements in RF circuits.

This paper presents the results of the development of a metal core substrate design which has advantages over conventional competitive designs. The manufacturing flow developed in this work has fewer process steps, uses fewer materials and shows interfacial adhesion strength above industry requirements.

The work outlines material evaluations to enhance the interfacial adhesion and corrosion resistance. The results of the evaluation of mechanical, chemical, and other methods to enhance interfacial adhesion are presented and compared. The enhanced interface shows significant adhesion increase for the circuitry metal over and beyond industry requirement.


Formation of conductors on a substrate can be achieved by dispensing conductive materials on its surface. The quality and reliability of these conductors depends upon the ink characteristics, substrate characteristics and the dispensing parameters.

In this study, two materials were dispensed on a substrate commonly used in the industry at various temperatures. Results of the effect of substrate temperature on the quality of conductors dispensed on it are presented. The line width, its cross section area and its resistance and resistivity were measured at increasing
temperature of the substrate and correlated to the substrate temperature.


Fine round and oblong features were printed using fine solder paste. Diameters and spacings were measured and data was analyzed to show solder feature printing capabilities. The printed features varied from 50 to 450 micron diameters with 50 to 150 micron spacings. Analysis of the solder features showed that printing of round features was possible at every size and spacing, with minimal bridging of the very small spaced features after reflow.


Use of very thin wafers in the semiconductor industry poses handling challenges during manufacturing. The goal of this study was to determine whether applying thin coatings could create stronger, easy to handle wafers. Standard three-point bend testing of coated and uncoated thin wafer samples was used to determine whether the coating strengthened the wafers to improve their handling properties. Data indicated that only the thinnest coating on the thinner silicon increased the peak break strength in three-point bend testing.


Conventional printed circuit boards (PCBs) may be replaced by thinner metal core boards for some applications, as well as for package substrates. Using thin, metal core technology may provide advantages for radio frequency (RF) circuits and packages, and increase heat dissipation for high power applications.

The metal core technology has several layers including the metal core; electro coated dielectric, sputtered metal layers, and electroplated copper. Especially for RF application and automotive electronics printed circuit boards with a metal core is gaining interest. The advantage of metal core PCB is the low thermal coefficient as well as the possibility to achieve a high density of vias and electronic component assembly.

This paper describes the realization of metal core PCB with a dense array of vias and with a low thermal coefficient. The dielectric layer is applied after vias have been formed providing a high density electronics assembly on a double sided PCB which exhibits the heat dissipation of a metal core with minimal thermal expansion. After photo chemically etching an array of vias, the metal core can be optionally plated with copper. The insulating dielectric is applied using a highly reliable electrodeposited coating. Metal core substrate provides the opportunity to form a via to the metal core to provide electrical grounding. The final traces are fabricated on top and bottom and can be interconnected through via openings.


Fabrication of tall features using selective electro deposition is well known process and has several
applications in microelectronics packaging. The use of conventional exposure and development processes is limited by the aspect ratio and sizes of the features obtained. This paper describes a novel approach to fabricated tall structures featured in thick photoresist. Tin and copper tall structures were made by selective electro deposition. Also presented are results from experiments performed to fabricate tall tin and copper pillars with nearly vertical walls on bare dices to form interconnect.


With the expansion of the use of sensors in everyday life, especially in medical and security fields, it has become pertinent that a substrate be chosen which is not only compatible with the sensor functionality and its manufacturing flow but also with the use environment of the sensor. Roll-to-roll manufacturability is also an important consideration along with the quality, reliability and cost of the end product. Material advances have provided a wide variety of choices which need to be studied and understood for competitive applications.

In this study, a sample of the results of the evaluation of selected substrate materials is presented. This effort helps provide a reference database and comparison to choose a material for a particular application and application environment.


A half century has passed since underfill was first applied to flip-chip ICs. In that time, much effort has been directed toward optimizing thermo-mechanical properties such as viscosity, stiffness, thermal expansion, and adhesion in order to make the underfill process as cheap, effective, and factory-friendly as possible. In recent years, attention has turned to increasing the thermal conductivity as a means of reducing IC temperatures in high-power devices.


In many applications, power is a controlling factor for size and cost. With increased demand for portable electronics like laptops, cell phones, and MP3 players that are smaller and flatter, the demand for thin and small form factor power sources has also risen. CNSE, therefore, explored commercially-available batteries with focus on thin-film batteries and small form-factor batteries. In order to gain understanding of the design, layout and the materials considerations, a battery deconstruction study was carried out. The main interest in looking at the construction of these batteries was to understand how the different layers had been deposited on the flexible substrate. Another objective was to attempt to identify the different components of the battery. There was interest in obtaining information about the specific components that are used to prepare the electrode materials.

“Developing acid copper plating capability on a new novel dielectric for a short term research project,” Greg Strommen, Kevin Mattson, Bernd Scholz, Syed Ahmad, Aaron Reinholz, Matt Noah, Josh Adamek, Jason Thomas, Tirosken Fonseka, Tharaka Chandanayaka, Lauren Tollefson, Matt Indihar, and Andrew Honeyman. 6th International Conference on Device Packaging, March 8-11, 2010. Scottsdale/Fountain Hills, AZ.
Acid copper plating is a very useful and cost effective process in the electronics industry for use as a conductor. Ongoing research continues to strive for quality plated films on a vast array of base material substrates and insulating dielectric layers. As part of an investigation to improve adhesion of plated copper to a novel dielectric material, an in-house copper plating system was setup to be able to control the plating process as necessary. A small scale copper plating system was designed to facilitate our research which would also be scalable to high volume manufacturing (HVM). Additionally, the set-up could be used for other studies, such as corrosion.


Thin, metal core substrates as system or package carrier have thermal and electrical performance advantages. Metal for the core has to fit the mechanical needs of the module. Carefully selected Fe/Ni compositions can fulfill custom needs for a system, package or module. But the iron in the Fe/Ni composition is susceptible to corrosion especially under high temperature, humidity, and pressure. Metal core substrates are typically coated with a dielectric layer before they can be put to use as high performance packaging substrates.


An array of accelerated temperature cycling (ATC) finite element (FE) simulations using ANSYS™, and drop-impact finite element simulations using LS DYNA™, are used to find the optimum elastic modulus and coefficient of thermal expansion (CTE) for a stacked chip scale package. For the ATC simulations, Anand’s constitutive model with properties for Sn96.5Ag3.0Cu0.5 (SAC305) and tin-lead eutectic (Sn63Pb37) are used for the solder joint. The strain energy density is used as a damage parameter to determine the number of thermal cycles to failure. Tri-linear elastic-plastic models are used for the solder joint properties in the drop-impact simulations. The maximum normal stress in the solder joints is used as damage parameter for the drop-impact simulations. Simulations show that the optimum underfill material has an elastic modulus of 2 GPa and a CTE of 25 ppm/K.


The objective of this project was to apply a self-assembly process in the development of a functional battery assisted passive (BAP) tag. A multifunctional sensor using RF signals was designed and fabricated. Multiple ASIC and OTS IC dice were placed in a multi-layer flexible carrier by applying a self-assembly method and packaged to archive inexpensive micro sensors. The interconnections were made using printable conductive inks to replace previously used thin film processes and to reduce costs. This flexible package consists of more than one polymer substrate with the devices embedded in it and connected to each other and are finally covered by polymeric planarization layers where the traces are printed on leading to the package terminal of the device.

The RF system can receive an RF signal, store the required info, and respond to stored information when prodded to do so through an RF signal. The flexible package consists of a polymer substrate with the device embedded in it and covered by a polymer. The polymer cover layer protects and sandwiches the
device between the substrate and itself. The interconnection from the chips to the package terminals is provided using vias in the cover-lay polymer. The package terminals on the cover-lay surface interconnect with the device through the vias in the cover-lay over the terminals on the device. Metallization is accomplished using a photolithography process.


Use of solder balls as component– and package-to-substrate interconnect media has proliferated with the increasing need for the miniaturization of electronic devices. Solder balls are either manufactured on the pads of devices or packages where they are needed or pre-manufactured individual solder balls are dispensed on the pads and reflowed to make a bump. Pre-manufactured solder balls require special equipment for manufacture, need tight tolerances, and thus are expensive. They come in standard sizes and are hard to obtain in custom sizes when needed.

A method is described to make custom-size individual solder balls using ordinary SMT equipment without special tooling. Ability to make custom-sized solder balls inexpensively can help expedite research and development projects with savings on total cost of the projects.


An Electroless Ni plating process for aluminum was evaluated and optimized, leading to smooth and uniform nickel growth approaching 28.2µm/hr. The effects of temperature, and process time were investigated. Nickel bumping die for solder adhesion was performed and the quality of the adhesion between the nickel and aluminum layers was evaluated.


Often the greatest cost for developing a new package or system is the acquisition of bare chips. To meet this challenge, a unique technique involving laser and plasma has been developed for extracting dice or chips for reuse and repackaging. Epoxy molded integrated circuit (IC) packages are decapsulated using a combination of a neodymium-doped yttrium aluminum garnet (YAG) laser and reactive ion etch (RIE) plasma etcher.

Using the parameters mentioned in this paper, a yield of over 70% of functional packages was achieved at the end of decapsulation.


Parallel stochastic self-assembly techniques are promissory process alternatives replacing common pick and place methods for small devices. Companies have adopted self-assembly techniques to place and fabricate microchips in high volume RFID devices. The objective of this study and process development was to enable the fabrication of IC chips for a parallel stochastic assembly process (PSAP) using components-off-the-shelf (COTS). Previously only custom designed IC chips or application-specific IC chips (ASIC) have been used in PSAP. A commercially available memory chip with rectangular form containing 8 I/O pads was used to test the concept in a RF micro sensor application. The chips were obtained in wafer form and the I/O pads were relocated into symmetrical arrangement by adding a redistribution layer (RDL) with vias to the original pads. A chip with simple shape, such as rectangle or square and symmetrically arranged pads will increase the PSAP yield while fully utilizing the economical benefits of the process; the chip orientation in the receptor site becomes irrelevant while its unique size and shape ensures that it settles in the correct place. This paper presents the design steps, processes, and materials used in the fabrication of redistribution layer for off-the-shelf IC components.


Engineering a single package housing multiple chips stacked vertically one above the other is a common practice that results in smaller and more efficient packages for devices. This article describes a case history and the challenges faced in the design and manufacture of the package


Drop testing is performed on stacked chip scale packages in eight configurations, including the use of two types of commercially available underfills. Full failure analysis using techniques such as dye penetrant and scanning electron microscopy (SEM) is performed. Corresponding explicit finite element simulations are performed using ANSYS® LS-DYNA. These simulations are used to determine a suitable damage parameter and consequently, drop test life correlations are constructed. Considerable differences in drop impact reliability between Sn63Pb37 and SAC305 solder are observed.


Interconnection and metallization integrity issues were encountered during the development of a flexible package for use in an RF system. The RF system can receive an RF signal, store the required info, and respond to stored information when prodded to do so through an RF signal. The flexible package consists of a polymer substrate with the device embedded in it and covered by a polymer. The polymer cover layer protects and sandwiches the device between the substrate and itself. The interconnection from the chip to the package terminals is provided using vias in the cover-layer polymer. The package terminals on the cover-layer surface interconnect with the device through the vias in the cover-layer over the terminals on the
device. Metallization is accomplished using a photolithography process. Electrical testing, metallography and SEM observation were used to identify the causes of interconnection issues. In response to interconnect quality challenges, the layout of traces on the package was redesigned and via formation process was modified. The processes and analysis techniques leading to the elimination of anomalies encountered during the prototyping of the package are discussed.


Setting up a modern facility for wafer-level fabrication, chip-scale packaging and surface mount technology far from the center of semiconductor activity entails tough challenges and careful planning. This article relates some of the good, the bad and the Quasimodo-ugly experiences faced by the NDSU staff.


Moiré interferometry and finite element (FE) analysis are used to quantify the deformation of stacked chip scale packages under thermal and accelerated thermal cycling loads. Basic thermo-elastic material property measurements are made of the constituent materials and found to be in good agreement with published values. Visco-plastic FE-based solder joint fatigue simulations indicate good reliability for several common design configurations of stacked packages.