Strong Coupling (Crosstalk) Between Printed Microstrip and Complementary Split Ring Resonator (CSRR) Loaded Transmission Lines in Multilayer Printed Circuit Boards (PCB)

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***Abstract*— The coupling between a microstrip transmission line (TL) and a complementary split ring resonator (CSRR) loaded TL in a multilayer printed circuit board (PCB) is investigated in this paper. More specifically, how well analytical expressions derived from single cell layout simulations compares with schematic simulations and PCB measurements of a multi-unit cell layout. The power radiating off the PCB was measured as well. This work paves the way for future development of guidelines for reducing the effects of coupling between CSRR loaded TLs and other microstrip TLs.**

***Index Terms*— Coupling, crosstalk and complementary split ring resonator transmission lines, multilayer**

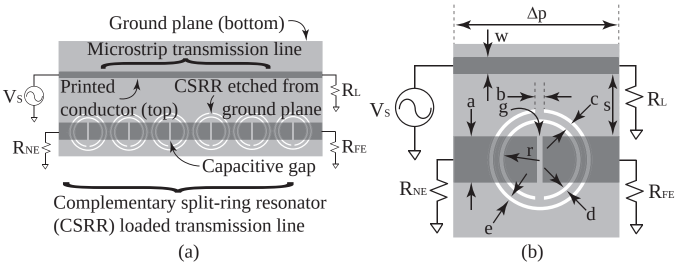

Fig. 1. (a) Strong-coupled microstrip and CSRR loaded transmission lines and (b) the unit-cell of the strong-coupled transmission lines.

I. INTRODUCTION

Modern RF devices are increasing in functionality while being required to operate in size limiting spaces. To reduce the overall footprint of RF electronics, designers are turning to new topologies with unique propagating characteristics. One such area includes printed transmission lines (TLs) with left-handed propagation which have the properties of positive and negative phase constants, shorter group delays and compact size [1] - [2]. Because of these features, left-handed TLs have been used to develop zero-phase networks [3], asymmetric power dividers [4] and unique filters [5]. Many of these applications use the complementary split ring resonator (CSRR) TL topology shown in Fig. 1 (a). As applications for CSRR loaded microstrip TLs continue to grow, the trend of miniaturized electronics will naturally require these TLs to be located in close proximity to other electronic circuitry sharing the same printed circuit board (PCB). Because of this vicinity unwanted noise may be coupled to other parts of the PCB.

The coupling between printed microstrip TLs has been studied extensively and some of the early research on this topic can be found in [6] - [9]. The objective of this work is to expand upon these efforts and study the strong coupling between the microstrip and CSRR loaded TLs in multilayer PCB applications. Specifically, the affects that a driven microstrip line may have on the properties of a CSRR TL are of interest. The strong-coupled TLs will be evaluated by dividing each TL into unit-cells of length, sources, and loads as shown in Fig. 1 (b). Then, each strong-coupled unit-cell will be modeled as a per-unit equivalent circuit. From this circuit, the analytical expressions derived from methods shown in [9] will be used to validate the seven-unit coupled voltages on the CSRR TL.

This paper differs from previously published work on printed CSRR TLs for the reason this problem is considered from an EMC point-of-view and not an intentional coupling problem as found in other compact power divider work [4]. In addition, initial results on the weak coupling between a printed microstrip TL and a composite right-/left-handed TL (CRLH TL) were recently published in [8]. That work presented results on the propagation behavior of CRLH TLs and the crosstalk due to various CRLH TL geometries and spacing that could be modeled as weak coupling. The research presented in this paper uses the analytical methods shown in [9] and contrasts by applying it to a three layer PCB. It will be shown these methods are accurate in their estimation when compared to simulations and measurements. The results will provide the groundwork for further experimentation of the coupling effects of a CSRR TL.

II. STRONGLY COUPLED MICROSTRIP TL AND CSRR TL IN THREE LAYER PCB

As shown in [9], the multi-cell CSRR TL equivalent circuit can be modeled by connecting several identical per-unit TL models in series. The single cell strongly coupled equivalent circuit model for a CSRR TL in parallel with a microstrip TL can be seen in Fig. 2. L_G and L_R denotes the series inductance of their respective TLs. C_L represents the series capacitance of the CSRR TL due to the gaps in the line. C_{GR} and L_{GR} are the mutual inductances and capacitances between the CSRR TL and microstrip TL. The parasitic capacitances between each line and the ground plane are C_C and C_G. L_L and C_R are there to model the effect of the CSRR ring topology that is etched in the ground plane. The source and load impedances are represented by R_S and R_L respectively. The CSRR TL is loaded at the near end with R_{NE} and with R_{FE} at the far end. Equations were derived from this circuit model and are shown in [9]. This equivalent model was used as a base for all multilayer layer designs. The circuit and equations were adapted accordingly to account for changes in the layout.

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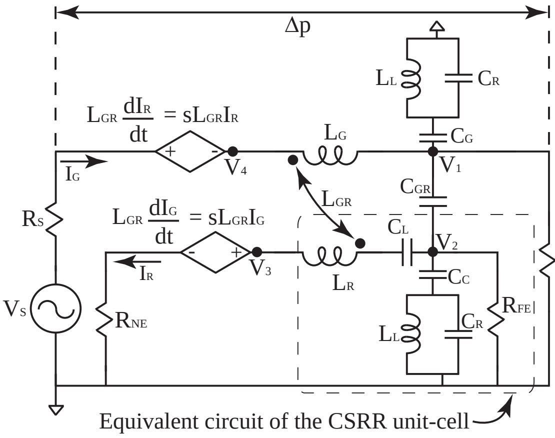

Fig. 2. The per-unit equivalent circuit of the unit-cell of coupled microstrip and CSRR TLs.

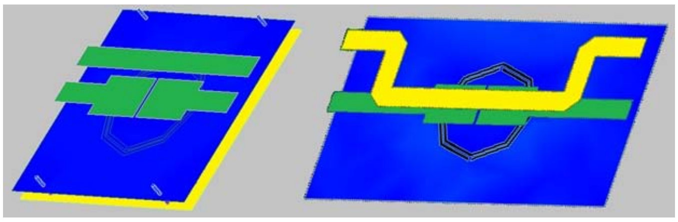

Fig. 3. A single cell model of the second ground plane on the left and the stacked microstrip TL on the right.

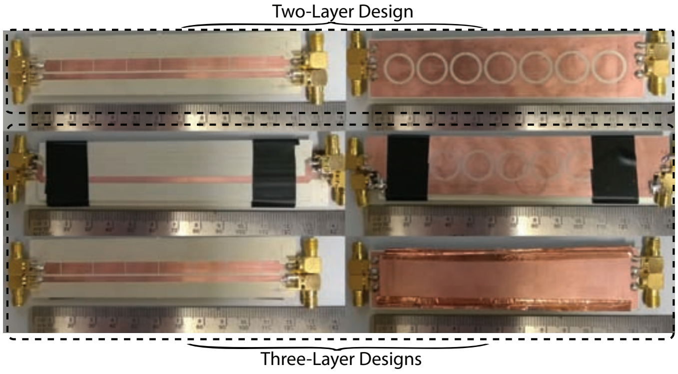

Fig. 4. Side by side of the top and bottom planes of the three tested PCBs. The top picture is the two layer, middle is the three layer stacked microstrip, and bottom is the three layer with a second ground plane.

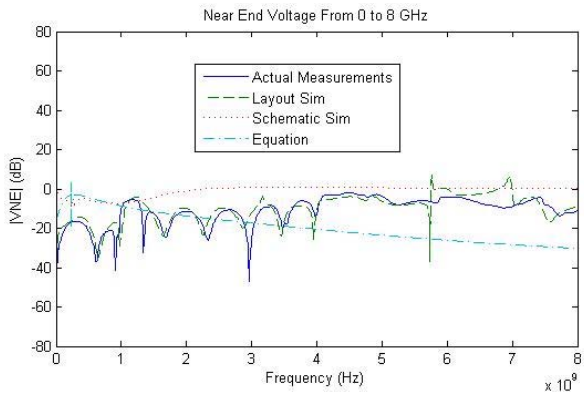

Fig. 5. Near end voltage comparison of the two Layer PCB.

The designs were to represent worst case scenarios of a realistic multilayer PCB layout. All three were manufactured and tested on 1.52 mm Rogers TMM4 substrate (ε = 4.5, $\tan\delta$ = .002) [11]. A seven cell two layer PCB was used as a control. The 50Ω microstrip TL was placed 1 mm away from the CSRR TL. The dimensions of the design are: w = 2.86 mm, s = 1.0 mm, a = 5.58 mm, b = 0.37 mm, c = 0.24 mm, d = 0.41 mm, e = 0.41 mm, g = 0.35 mm, Δp = 24.35 mm, r = 5.96 mm. All three PCBs used these dimensions for the CSRR TL. Fig. 3 shows a single cell of the two three layer designs. The second ground plane layout is identical to the two layer board with an added third layer beneath the CSRR TL ground plane. This was done because there was a concern with the circular cuts is the ground plane beneath the CSRR TL. These might cause unwanted coupling with other copper planes below. The strong coupling model was not changed for this design since the added plane was thought to have negligible effect on the strong coupling on the top layer. In ADS Momentum simulations[10], the two ground planes were attached using picketed vias 5 mm away from the board edge space 12.2 mm apart. For testing, the second ground plane was attached with copper tape. The three layer stacked PCB has the microstrip TL directly above the CSRR TL. In the equivalent circuit model, C_G and the inductor/capacitor pair were removed as it was assumed these would be negligible through the two layers of dielectric.

III. SIMULATIONS, MEASUREMENT, AND VALIDATION OF RESULTS

The two primary focuses of this paper are to validate the strong coupling model as shown in [9] and to compare the various layouts and their results. There are four separate results for each PCB. All designs were first tested in ADS Momentum [10] to find the near end voltage. The seven cell layout was created and the simulation results were recorded. The PCBs were manufactured from these layouts. The tested boards are shown in Fig. 4. The single cell ADS Momentum layout was simulated and the equivalent circuit parameters were extracted using the methods presented in [9]. The values were placed in the equations also shown in [9] and the near end voltage was calculate analytically. These equivalent circuit values were also placed in the seven cell ADS schematic and simulated. Fig. 5, Fig. 6, Fig. 7 shows the comparison of the four results for all three layouts from 0 to 8 GHz. The layout simulation and PCB measurements were fairly accurate for every case. The equivalent schematic and analytical equations were off since they did not account for the resonances of the voltage. These findings are comparable to the ones from [9]. The other focus of this paper was to compare the three layouts from each other. Fig. 8 show the near end voltage measured from all the PCBs over the range of 0 to 8 GHz. The microstrip stacked had

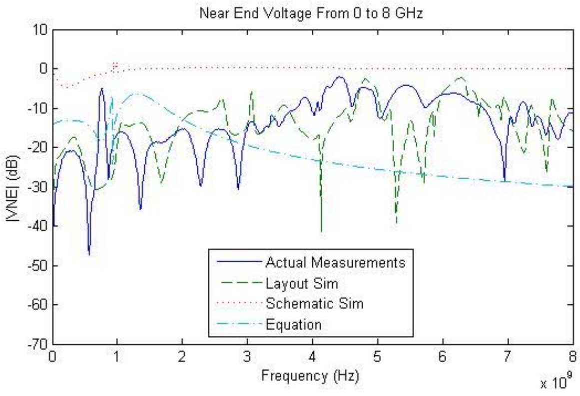

Fig. 6. Near end voltage comparison of the second ground plane PCB.

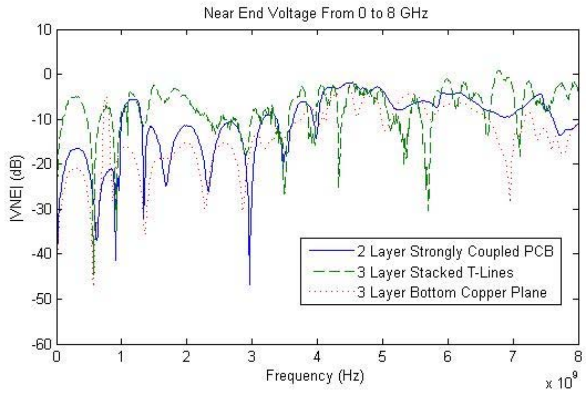

Fig. 8. Measured near end voltage comparison of the three PCBs.

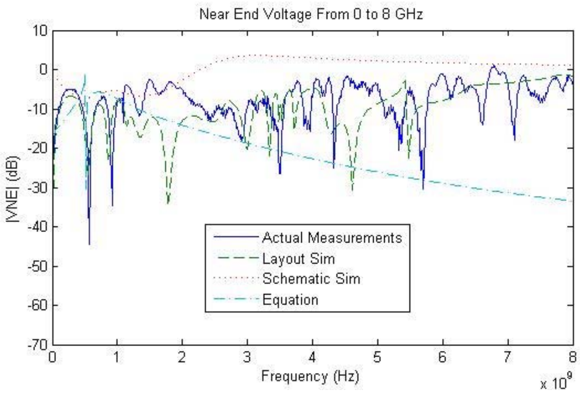

Fig. 7. Near end voltage comparison of the stacked PCB.

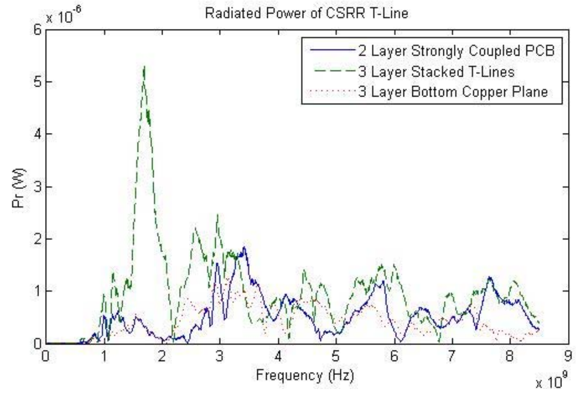

Fig. 9. Radiated power from below the ground plane with horn antenna 50 cm away and 10 dBm input power on the CSRR TL.

much higher near end voltages than the two layer control. This indicated the microstrip TL and CSRR TL are more strongly coupled when they are above one another than when they were side by side. Adding a second ground plane underneath the CSRR circles lowered the near end voltage. Therefore, the side by side transmission lines coupling is weakened when a second ground plane is added underneath the CSRR ground plane. This indicates that clever use of ground partitioning could possibly be used to reduce coupling.

IV. RADIATED EMMISSIONS OF CSRR TL

Each of the three designs were then tested to find the power radiating from the PCB. The CSRR TL was driven with a power input of 10dBm on one port and all other ports were terminated with 50Ω loads. The radiated field was then measured with a TDK horn antenna (HRN-0118). The field was measured below the ground plane at a distance of 50 cm. Fig. 9 shows the power measured at the antenna from 0 to 8.5 GHz. The peak power measured was around 6 μw with the stacked TL PCB. The difference between the two layer and second ground plane PCB was fairly minimal.

V. CONCLUSION

The strong coupling analytical expressions, equivalent circuit, and methods as presented in [9] can be applied to multilayer designs. Placing a microstrip TL above a loaded CSRR TL can result in a noise voltage increase of 10 dB. Placing and via stitching a ground plane below the CSRR ground plane can reduce coupling effects by 5 dB. The placement of the microstrip TL nor the addition of a second ground plane had a large effect on the radiating power above 3 GHz. This further demonstrates that special layout considerations must be applied when designing a CSRR TL.

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