A Low Power CMOS Technology Compatible Non-volatile SRAM Cell

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ABSTRACT

This paper presents a CMOS technology compatible non-volatile 8T SRAM called NV SRAM. NV SRAM works as conventional 8T SRAM to keep high speed and high noise margin in work mode; in sleep mode, the data is kept in non-volatile part and the power supply is switched off, thereby minimizing the leakage energy without data loss. Based on 65 nm SMIC Technology, simulation results show that sleep time is longer than 219 μs, NV SRAM is able to achieve energy savings. The NV SRAM is particularly effective to implement on-chip-memories with long idle time.

INTRODUCTION

Static Random Access Memory (SRAM) has been the predominant technology used to implement memory cell in computer systems [1], which is volatile in nature; it means that the holding data is lost as long as power supply is cut off [2]. The CMOS-compatible memory cells are extensively applied, and their features predominantly affect the chip size, operational speed, and power dissipation of memory devices [3]. In on-chip memories, such as cache memories, the static energy or leakage energy is a dominant amount in total energy dissipation [2] [4]. And on-chip memories take over 50% of the die area according to 2012 ITRS [5]. These issues are expected to aggravate with continuous technology scaling, especially in battery-powered computing devices, such as laptop computers, smart phones, and medical sensors [6].

In this paper, a low power and CMOS compatible NV SRAM based ultra-low leakage energy hybrid memory system is developed. The leakage energy of NV SRAM is greatly reduced due to cutting off power supply in sleep mode and adopting non-volatile part to hold data. What is more, the proposed NV SRAM cell can be fabricated using conventional CMOS processes.

NV SRAM cell design

Figure 1 shows the schematic of proposed NV SRAM cell. It includes a conventional 8T SRAM cell, two CMOS transmission gates, a level shifter, and non-volatile part. Two CMOS transmission gates TG1 and TG2 control the data back up as the bridge from SRAM cell to non-volatile part. In order to achieve similar transmission speed of NMOS and PMOS transistors, the size (W/L) of PMOS is set as twice as that of NMOS. And the minimum size (W/L=120 nm/60 nm) for NMOS in 65 nm SMIC Technology is adopted to reduce the area overhead and increase transmission speed. The capacitor C2 is designed twenty times larger than capacitor C1, M1 and M2 have a similar size to C1, which is proved optimum in [8] for Fowler-Nordheim tunneling mechanism.

In work mode, both SLP and WAK are set to "0", transmission gates are cut off, the power for non-volatile part is off, and NV SRAM cell works as a conventional 8T SRAM cell, achieving fast access time, high noise margin, and high robustness to PVT variations [9].

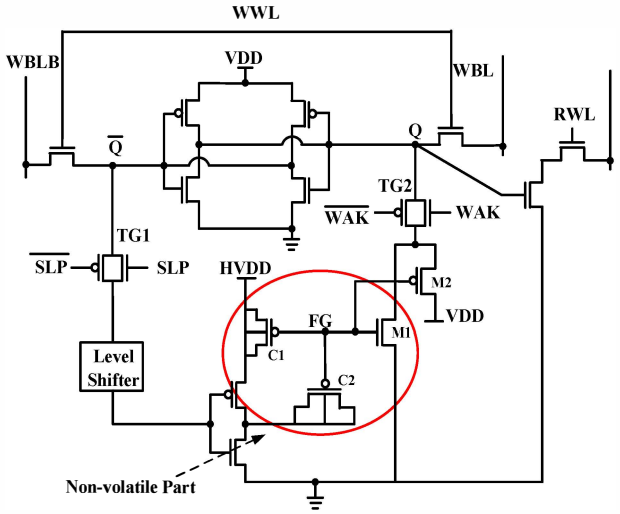

Figure 1: NV SRAM cell

Before the sleep mode, SLP is set to a short pulse and WAK is still "0". Simultaneously, charge pump provides a high voltage to HVDD to make non-volatile part work. If Q is "0", $\overline{Q}$ is "1", $\overline{Q}$ is shifted to a high voltage through level shifter as input to inverter. The electrons are removed from the floating gate (FG) by applying high voltage at the body of a small C1 while keeping the body of a large C2 grounded. FG is "1". Otherwise, FG is injected electrons which are assisted by hot carriers at drain node of NMOS M1. In the sleep mode, SLP and WAK are still "0", data is held in non-volatile part to achieve energy savings.

Finally, the SRAM is ready to return to the work state while SLP keeps "0", WAK provides a short high pulse to open the TG2, and NV SRAM cell is power-on. If potential of FG goes higher than the threshold voltage of

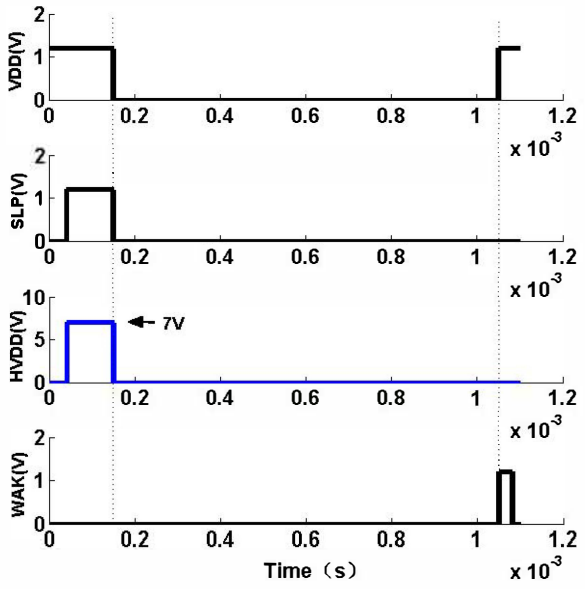

Figure 2: Timing of the backing up and restoring data processes

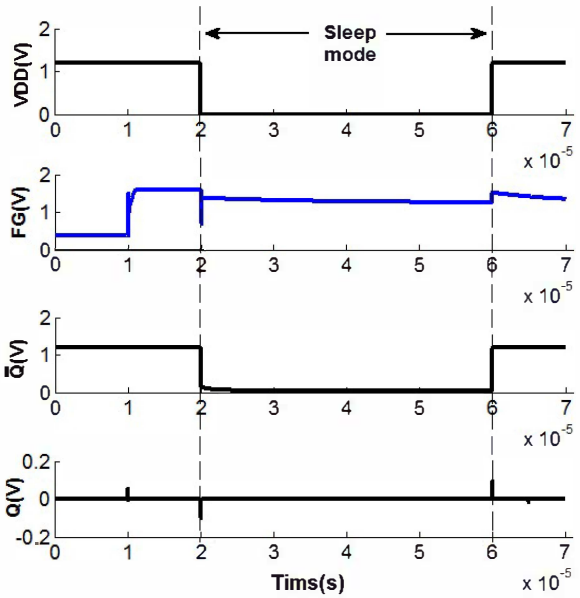

Figure 3: Simulation results of work and sleep operation of NV SRAM cell

M1, Q is pulled down to "0", data in NV SRAM cell is "0"; otherwise, Q is pulled up to "1", data in NV SRAM cell is "1".

Simulations are performed based on 65 nm SMIC Technology with 1.2 V power supply. Figure 2 shows the backing up and restoring data processes of NV SRAM cell. Although the voltages of the level shifter and HVDD are different, they have the same pattern with time. HVDD is 7V provided by charge pump, following the Fowler-Nordheim tunneling mechanism, as given by

$$J_{F-N} = AE_{OX}^2 \exp\left(-B / E_{OX}\right) \quad (1)$$

Where J_{F-N} is current density, and E_{OX} is electrical field. Both A and B are constants. Since the Fowler-Nordheim tunneling is known to be a safe way to inject charge repeatedly through a thin dielectric film, 6V-8V is desired to be applied across the tunneling oxide for charge injection [8] [10]. Finally, 7V is proved optimum level of HVDD by simulation results.

Simulations

Figure 3 shows simulation results that NV SRAM cell holds "0". Before the sleep mode "0" is held in NV SRAM cell, "0" is restored again by non-volatile part after sleep mode. The measured FG voltage is plotted as a function of non-volatile part to control transistor M1 or M2. The FG is deprived of electrons by tunneling current before the sleep mode, and FG keeps constant in sleep mode. When the power is supplied, FG potential is sufficiently high to successfully open the M1 that pulls down Q node.

To investigate the energy efficiency of NV SRAM, the energy dissipation of NV SRAM cell and conventional 8T SRAM cell are compared, as shown in figure 4. Because the power of NV SRAM cell is cut off in sleep mode, and the power of lever shifter and HVDD are supplied at the process of data backing up, the most of energy dissipation is produced by non-volatile part and level shifter in Figure 4 (a). Figure 4 (b) shows the energy dissipation of conventional 8T SRAM cell, leakage power is the only power source of circuit in sleep mode. And the average power consumption is calculated, as shown in Table 1. The average power of NV SRAM cell is 19.814 nW, while the average power of conventional SRAM cell is 90.45 pW. It is calculated that the sleep time is longer than 219 μs, NV SRAM is able to achieve energy savings

TABLE I. AVERAGE POWER

	Different SRAM cell	
	NV SRAM cell	***Conventional SRAM cell***
Power consumption	19.814 nW	90.45 pW

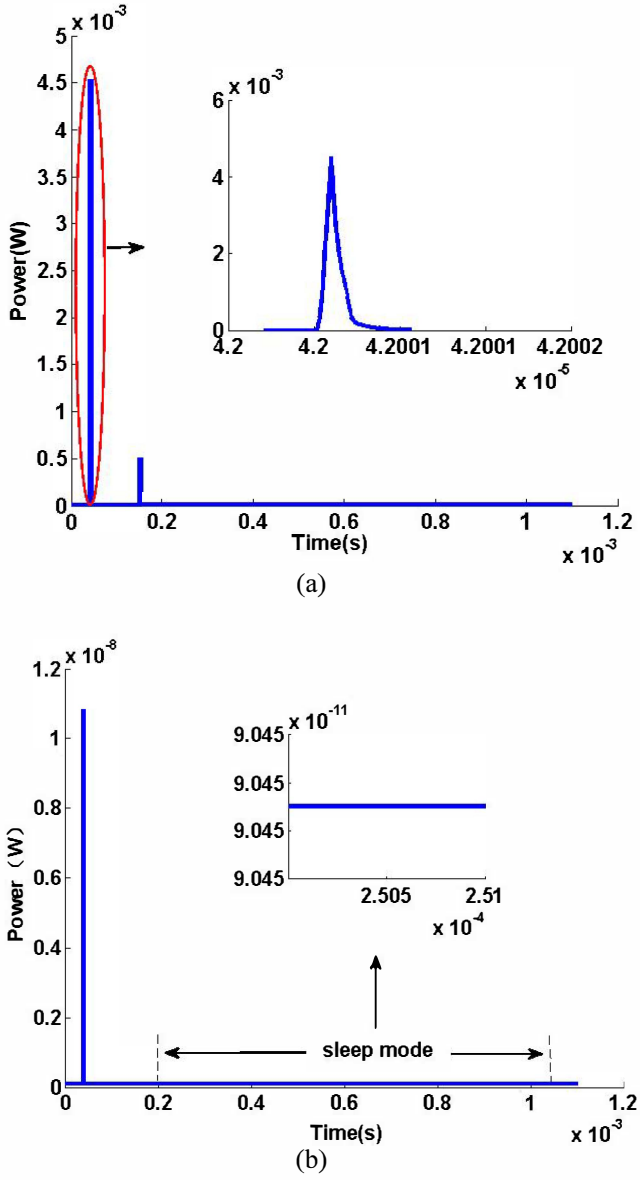

Figure 4: Energy dissipation comparison of (a) NV SRAM cell and (b) conventional 8T SRAM cell

Conclusions

This paper has presented a CMOS compatible NV SRAM cell. The proposed technique uses conventional 8T SRAM in work state for fast operation; before the sleep mode, it backs up data with non-volatile part; in sleep mode, it switches off the power supply to eliminate leakage energy. The impact of sleep time is analyzed in detail, and optimum sleep time is provided for NV SRAM cell. When the sleep time is longer than 219 μs, NV SRAM is able to achieve energy savings. It is concluded that NV SRAM is more advantageous in on-chip memories with long idle time.

ACKNOWLEDGEMENTS

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