NOVEL CMOS SRAM VOLTAGE LATCHED SENSE AMPLIFIERS DESIGN BASED ON 65 nm TECHNOLOGY

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ABSTRACT

A novel voltage latched sense amplifier is proposed in this paper. It applies a self-closing bit-line module technique, which makes the input and output nodes separated to optimize sensing delay and power consumption. Initially, the size of transistors in the circuits is adjusted to speed up the circuit and lower the power. The simulation results show that the proposed design improves sensing when smaller bit-lines difference requires for full-swing amplification as the conventional voltage latched sense amplifier. The proposed design also improves power efficiency at least 30% as compared to the conventional voltage latched sense amplifier.

INTRODUCTION

SRAM stands for Static Random Access Memory, a volatile memory that remains the content as long as the power is supplied [1]. The sense amplifier operates only during read into memory phase.

One of the elements of the data-path in an SRAM design is the sense amplifier. The sense amplifier activated during a read operation is used to sense the voltage differential on the bit-lines at its input, and generate a full-rail voltage swing at its output (Figure 1) [1]. The memory take it quickly either as '1' or '0' rather than trying to calculate or wait for its voltage full swing level, thus saves time in read operation [2].

In advanced memories, the capacitance of the bit-line is increasing due to technology scaling and the increasing number of cells attached to the column [3]. Because of this increasing capacitance, the conventional voltage latched sense amplifier cannot keep their performance [4].A novel voltage latched sense amplifier is proposed to reduce the sense circuit delays. The proposed voltage latched sense amplifier provides self-closing bit-line module that reduce the bit-line capacitance, and has the ability to quickly amplify a small differential signal on the bit-lines *(bit, bitb)* to the full swing level without requiring a large input voltage swing. The self-closing bit-line module is used as one of the most effective ways to reduce both sensing delay and power consumption of the SRAM. The following sections compare the conventional voltage latched sense amplifier (VLSA) and the novel voltage latched sense amplifier (VLSA-I), and it is extensively simulated and tables presented in comparison with the VLSA and VLSA-I.

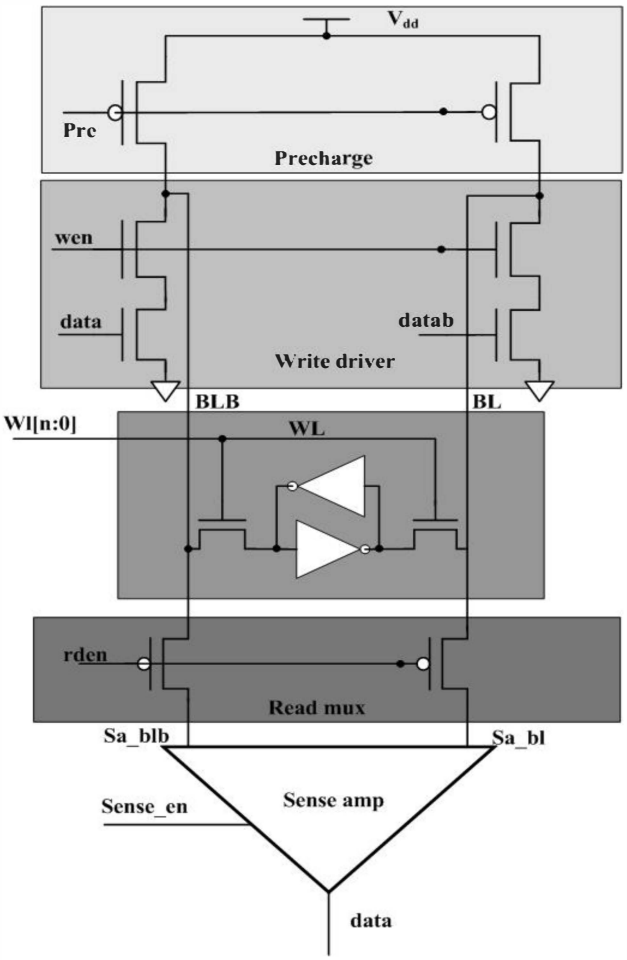

Figure 1: Basic schematic of one column for small signal memory array using 6T cell

A CONVENTIONAL VOLTAGE LATCHED SENSE AMPLIFIER

Figure 2 shows the VLSA design based on SMIC 65 nm technology. M1, M3, M2, and M4 form the inverters that resolve the differential voltage on the bit-lines to a full-swing at the output. The internal nodes of this design are pre-charged through the bit-lines. The circuit design operates directly based on the voltage differential developed on its internal nodes by the input bit-lines. When the word-line is turned on and priors to the triggering of the sense amplifier, M7 is off and pass transistors M5 and M6 are on. As the differential develops on the bit-lines, the

Δbit on the internal nodes of the sense amplifier has enough voltage difference. When the sense signal *sen* is asserted, the cross-coupled inverters consist of M1, M3, M2, and M4 amplify this differential voltage to its full-swing output.

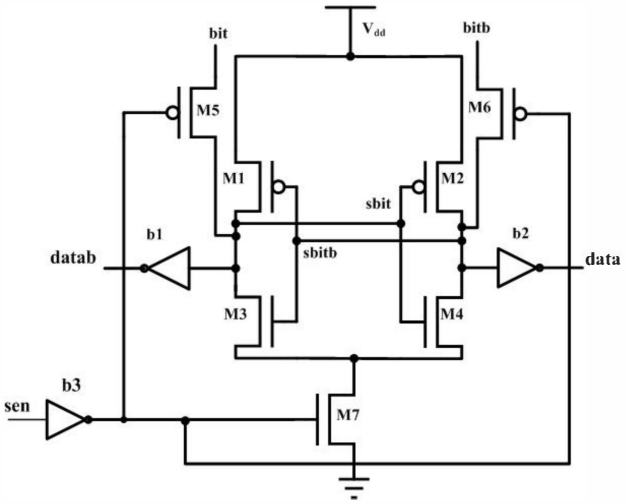

Figure 2: Voltage latched sense amplifier (VLSA) circuit

A NOVEL VOLTAGE LATCHED SENSE AMPLIFIER

Figure 3 shows VLSA-I design. The circuit is mainly based on VLSA style, and added self-closing bit-lines module which is consist of MOS transistors M6, M7, M10, and M11. The self-closing bit-line module is used for transmission and turning off the voltage. When the control signal PRC is a high level, the sensitive amplifier is off. Pre-charge transistors M12 and M13 are turned on. The sensitive amplifier enters into a pre-charge state. Two nodes *output1* and *output2* discharge to the "0" potential by two NMOS transistors M12 and M13, so the pre-charging process do not consume energy. In the pre-charging process, the balance transistor M5 is turned on, and the two outputs are at the same potential before the sensitive amplifier works. When two nodes potential *output1* and *output2* are "0", self-closing bit-line module of two PMOS transistors M6 and M7 are turned on. The bit-lines (*bit*, *bitb*) voltage transfers to the gate M9 and M8 transistors through M6 and M7.

When the control signal PRC is low. The power supply voltage of V_{dd} charges the two outputs by the conductive Ml and M2 transistors. Then M8 and M9 are turned on, two output terminals of the sensitive amplifier are respectively to discharge through M8 and M9.Two nodes potential of *output1* and *output2* rise or fall depend on the power of V_{dd} by the charging of outputs speed and the discharging of outputs rate. In the beginning, the charging current is greater than the discharge current, so the potential of two points (output1, output2) rise. Because the potential for bit-lines (*bit*, *bitb*) are not the same, so the *Δbit* on the internal nodes of the sense amplifier has enough voltage difference, when the cross-coupled inverters consist of M1, M3, M2, and M4 amplify this differential voltage to its full-swing output. When the *output1* or *output2* increases to a certain voltage, and the positive feedback between the pass transistors (M8, M9) and the self-closing bit-line module is formed. The M6 or M7 is turned off, and the self-closing bit-line module is operated to reduce static power consumption.

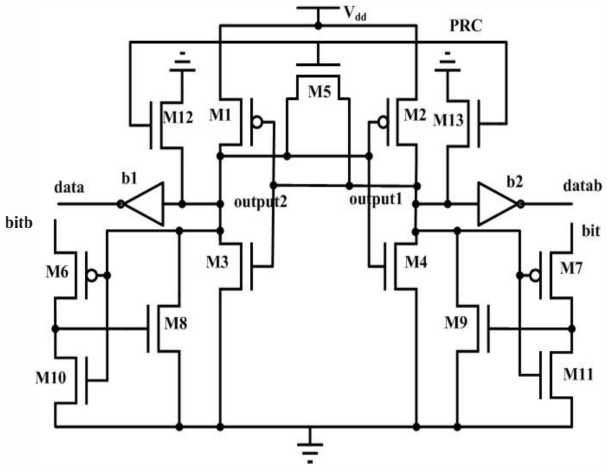

Figure 3: Novel voltage latched sense amplifier (VLSA-I) circuit

SIMULATION RESULT

A. Delay time

Based on 65 nm SMIC technology, the simulation is performed to compare the delay time of the two sense amplifiers. As for VLSA circuit, the input and output nodes share sensitive amplifier that can increase capacitance which extend the production time of the bit-line signals difference. In addition, when the sensitive amplifier in amplification phase, the bit line capacitance and the I/O circuit of input capacitance are used as the sensitive amplifier load, to affect the discharge time, and reduce the speed of amplification, while increase power consumption. The novel voltage latched sense amplifier applies a self-closing bit-line module technique, which makes the input and output nodes separated. It reduces the total capacitance.

Table I and Table II show the delay time influenced by the bit-line signals difference. It shows that the VLSA-I amplifies the small bit-line signal (0.2 V) faster by 15% than the VLSA. With the increase of the small bit-line voltage, the delay time decreases. The delay time of VLSA is reduced by 9% with the *Δbit* increase. The delay time of VLSA-I is reduced by 23% with the Δbit increase. Obviously, the delay time of VLSA-I is smaller than that of VLSA.

Table I The Δbit of VLSA affected delay time with the three different process corners

Δbit(V)	VLSA, 1.2 V_{dd}, 200MH freq,(0-1) bit		
	td(ps)_ff	*td(ps)_tt*	*td(ps)_ss*
0.1	170	181	195
0.2	164	173	184
0.4	158	167	176
0.6	157	165	175
0.8	157	164	174

Table II The Δbit of VLSA-I affected delay time with the three different process corners

Δbit(V)	VLSA-I, 1.2 V_{dd}, 200MH freq,(0-1) bit		
	td(ps)_ff	*td(ps)_tt*	*td(ps)_ss*
0.1	160	176	186
0.2	133	148	158
0.4	114	123	142
0.6	104	115	113
0.8	103	113	125

B. Total power consumption

The power of both sense amplifiers is also simulated. Since the input and output nodes are separated, the total capacitance of VLSA-I and number of transistors decreases, which results in the power consumption reduction.

Table III and Table IV present the total power consumption of two sense amplifiers with the change of the bit-lines signal difference. Table III shows that the power of VLSA increases with the Δbit enlarging, but Table IV shows that the power of VLSA-I decreases with the Δbit increasing. And the power of VLSA-I is reduced by 34% than the power of VLSA with the small bit-line signal about 0.2V. It means that VLSA-I improves power efficiency.

CONCLUSION

The novel voltage latched sense amplifier applies a self-closing bit-line module technique, which makes the input and output nodes separated to decrease the total capacitance. The proposed design has the ability to quickly amplify a small differential signal on the bit-lines (*bit*, *bitb*) to the full swing level without requiring a large input voltage swing. This novel voltage latched sense amplifier helps reduce both power consumption and sensing delay, especially in large size SRAM design. Thus it is concluded that the self-closing bit-line module technique is suitable for applications where low-voltage, low-power, high-speed, and stability are crucial design considerations. The simulations results clearly show the advantage of the VLSA-I design over the VLSA design.

Table III The Δbit of VLSA affected total power with the three different process corners

Δbit(V)	VLSA, 1.2 V_{dd}, 200MH freq,(0-1) bit		
	P(uw)_ff	*P(uw)_tt*	*P(uw)_ss*
0.1	12..9	12.7	12
0.2	12.7	12.5	11.8
0.4	13.4	13	12.4
0.6	14.5	14.1	13.4
0.8	16.1	15.2	14.5

Table IV The Δbit of VLSA affected total power with the three different process corners

Δbit(V)	VLSA-I, 1.2 V_{dd}, 200MH freq,(0-1) bit		
	P(uw)_ff	*P(uw)_tt*	*P(uw)_ss*
0.1	10.6	9.3	7.7
0.2	9.3	8.3	6.9
0.4	8.3	7.3	6.1
0.6	7.8	7	5.9
0.8	7.7	6.8	5.1

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