# ANALYSIS AND DESIGN OF CMOS CHARGE PUMP FOR EEPROM

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## ABSTRACT

A CMOS charge pump circuit, which can be applied in electrically erasable programmable read-only memory (EEPROM), is introduced in this paper. The performance including output voltage, rise time, power as well as changing pattern of output voltage versus load current of the traditional Dickson charge pump (TDCP), improved charge pump (ICP), and second improved charge pump schematic (NCP-2) are analyzed and compared. The simulation results show that the output voltage of NCP-2 is higher than other two charge pump circuits in three process corners. Meanwhile, the power consumption of NCP-2 is also much higher than other two circuits.

## INTRODUCTION

As read and write operations are the core function of EEPROM, the charge pump circuit that generates high voltage for reading and writing plays a significant role in the whole system [1]. The high programming voltage from charge pump is used to realize data storage or erasure by injecting electrons into or extract electrons from floating gate or floating gate-like device in non-volatile memory [2].

In EEPROM, charging and discharging electrons on the floating gate by F-N tunneling effect is the approach to achieve data storage [3]. The intensity of the electric field in tunnel oxide layer has to reach a certain value in order to produce effective tunneling current. J. Dickson proposes the earliest charge pump circuit [4], which is still the basis of a fair fraction of current charge pump circuit design.

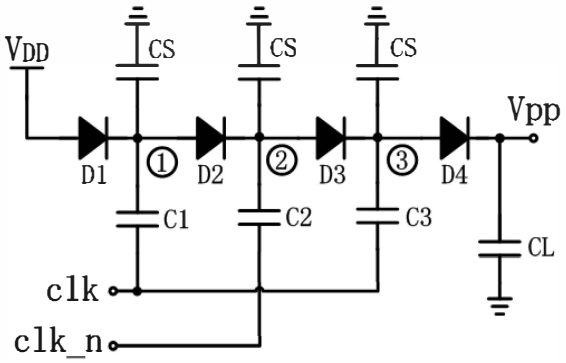


*Figure 1: The schematic of traditional Dickson charge pump*

Figure 1 shows a schematic of a 3-level of traditional Dickson charge pump (TDCP). The charge pump enhances the output voltage through transferring charges stage by stage [4]. The internal node voltage gets higher after charges are pushed from the previous stage through alternated clock signals; hence a high voltage can finally be obtained at the output node.

The output voltage, $V_{PP}$, can be described by the following expression [5]:

$$V_{PP} = V_{DD} + N[(\frac{C}{C+C_S})*V_C - V_D - \frac{I_{PP}}{(C+C_S)*f}] - V_D \quad (1)$$

where $V_{DD}$, $N$, $C$, $C_S$, $V_C$, $V_D$, $I_{PP}$, and $f$ are power supply voltage, number of stages, coupling capacitance, parasitic capacitance, clock amplitude, voltage drop of conducting diode, output current, and clock frequency, respectively.

As can be seen from the expression (1), the output voltage is mainly affected by four factors: the supply voltage, the number of stages, the clock frequency, and the ratio between coupling and parasitic capacitance.

## IMPROVED CHARGE PUMP CIRCUITS

In actual design process, the diode is replaced by a MOSFET with gate and drain connected together. $V_D$, the threshold voltage of the MOSFET, can be expressed as [6]:

$$V_D = V_{D0} + \gamma(\sqrt{2|\varphi_F| + V_{SB}} - \sqrt{2|\varphi_F|}) \quad (2)$$

where $V_{D0}$, $\gamma$, $\varphi_F$ and $V_{SB}$ are the intrinsic threshold voltage, body effect coefficient, surface potential, and the source-bulk potential difference, respectively.

The equation above shows that $V_{SB}$ has a great impact on the threshold value as well as output voltage. If $V_{SB}$ could be adjusted lower, or to be zero theoretically, the threshold voltage is going to be substantially reduced, which results in an enhanced output voltage.

Figure 2 shows the schematic of improved charge pump (ICP). Take the first stage as an example: when *clk* is low, node 1 is at high potential while node 2 is at low potential; thus M1 and M2 are turned on simultaneously. Due to the fact that the drain of M2 is connected to the bulk of M1, $V_{DD}$ not only charges node 2 but also the bulk of M1 by the same amount, which leads to a higher bulk potential therefore a lower $V_{SB}$.

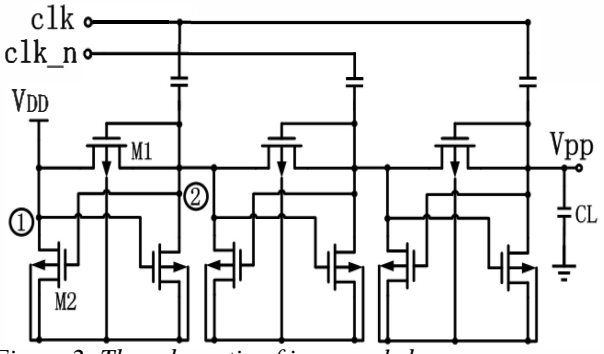

*Figure 2: The schematic of improved charge pump*

Figure 3 shows second improved charge pump schematic, named NCP-2 [7]. In this circuit, pass gate transistors MS1, MS2, and MS3 are used to transfer charges with much lower voltage drop across the transistor by feedback control.

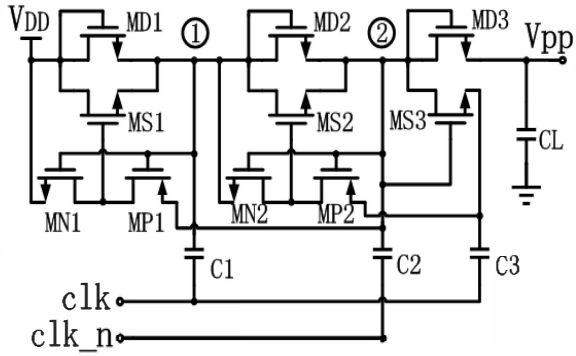

*Figure 3: The schematic of NCP-2*

The key difference compared to the other two circuits is that the gate of MS1 can be charged at a potential higher than $V_{DD}$ through MP1 from node 2; hence MS1 can be completely turned on and node 1 has a potential equals to $V_{DD}$ without threshold voltage loss [8]. The output voltage ($V_{PP}$) can be calculated by the following expression:

$$V_{PP} = V_{DD} + N[(\frac{C}{C+C_S})*V_C - \frac{I_{PP}}{(C+C_S)*f}] - V_D \qquad (3)$$

As illustrated before, the different from the expression (1) and expression (3) is that $N*V_D$ is dropped out in this equation since threshold voltage loss no longer exists. Consequently, the $V_{PP}$ of NCP-2 is higher than the $V_{PP}$ of traditional charge pump.

## SIMULATION RESULT

Based on TSMC 0.35 μm CMOS technology, three 12-stage charge pumps, including TDCP, ICP, and NCP-2 are implemented. The voltage amplitudes of *clk* and the *clk_n* are the same as the power supply voltage. The clock frequency and coupling capacitance are set at 20 MHz and 170 fF respectively. Besides, the size of transistors, load current, and the power supply voltage of three 12-stage charge pumps are same.

Figure 4 shows the simulation result of output voltages for the NCP-2 circuit under 3.3 V supply voltage. It can be observed that the worst case among all results in different process corners is higher than 15 V.

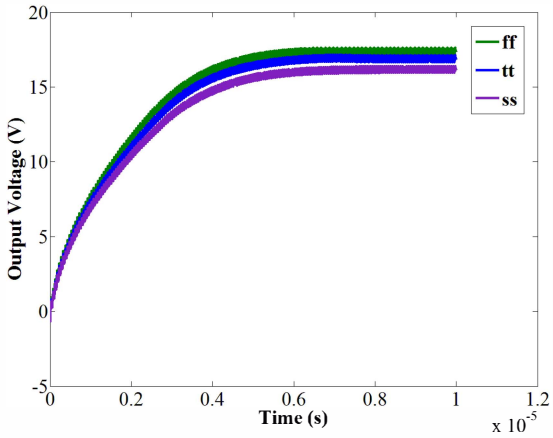

*Figure 4: The simulation result of output voltages for the NCP-2*

The load current of the circuit can affect the output voltage. As can be seen from Figure 5, the output voltages decrease with the increasing of load current from 0 μA to 6 μA for the NCP-2 circuit in three process corners. This relationship between output voltage and load current represents the load capacity of circuit.

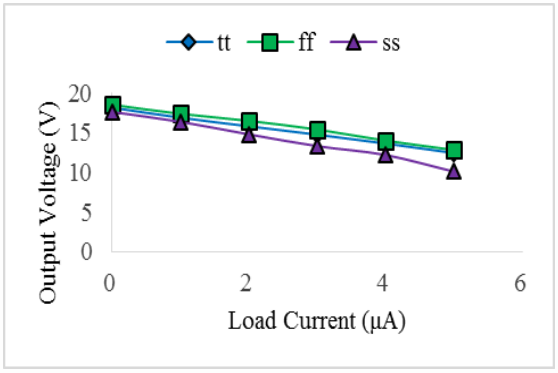

*Figure 5: The simulation result of output voltages versus load current*

Figure 6-8 show the simulation results of output voltages for the traditional Dickson charge pump and two improved charge pump circuits in three process corners. The power supply voltage in this simulation ranges from 1.8 V to 3.3 V. It is shown that there is a striking improvement for the output voltage as supply voltage rising.

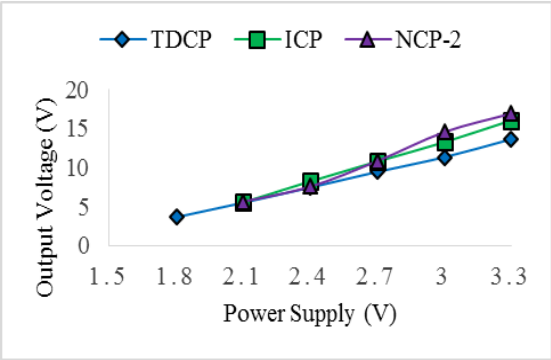


*Figure 6: The output voltages versus $V_{DD}$ in tt corner*

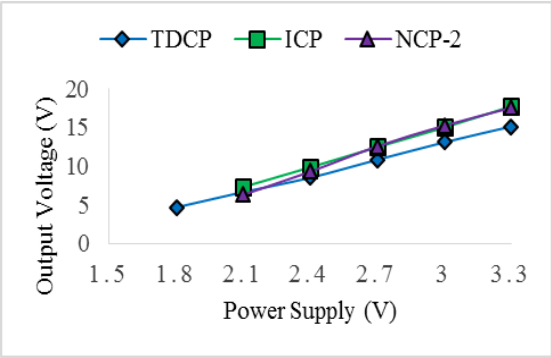


*Figure 7: The output voltages versus $V_{DD}$ in ff corner*

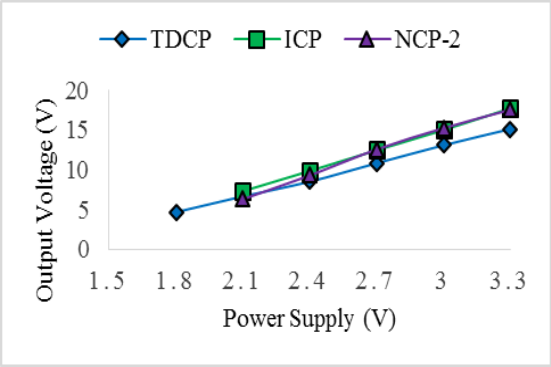


*Figure 8: The output voltages versus $V_{DD}$ in ss corner*

The power consumption of charge pump circuits in three process corners with 1 μA load current is summarized in Table I. It can be noticed that the NCP-2 circuit consumes much higher power than other circuits in exchanging for higher output voltage.

TABLE I. COMPARISON OF THE POWER CONSUMPTION

| process corners | The structures of circuit | | |
|---|---|---|---|
| | ***TDCP*** | ***ICP*** | ***NPC-2*** |
| tt | 0.163 mW | 0.152 mW | 0.289 mW |
| ff | 0.164 mW | 0.150 mW | 0.280 mW |
| ss | 0.162 mW | 0.154 mW | 0.282 mW |

## CONCLUSION

Three charge pump circuits have been introduced and analyzed in this paper. The load capacity of circuit is reflected in the output voltages decrease with the increasing of load current. The supply voltage has a great impact on the output voltage. From the simulation results of the output voltage versus $V_{DD}$, the output voltage of NCP-2 is higher than other two charge pump circuits in three process corners. However, the power consumption is also much higher than other two circuits. The NCP-2 circuit presented in this paper provides 16.94 V, 17.56 V, and 16.38 V in tt, ff, and ss process corners respectively, under 3.3 V power supply voltage. Although floating of the process leads to changes of the output voltage, it also satisfies the requirement of high programming voltage in EEPROM.

## ACKNOWLEDGEMENTS

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