NOVEL BIDIRECTIONAL IO MULTIPLEXING CIRCUIT DESIGN

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ABSTRACT

New bidirectional IO multiplexing circuits are presented in this paper. They are applied in the chips which consist of several modules, making the modules share the same IOs. The chip area therefore is saved by reducing the number of IOs. As compared with the unidirectional IO multiplexing circuits, it realizes bidirectional IO multiplexing among different modules. Taking the chip which consists of four modules as an example, the new IO multiplexing circuits based on static and dynamic CMOS circuit are compared and analyzed. According to the simulation results, the maximum operating frequency of new bidirectional IO multiplexing circuit reaches as high as 2.5GHz.

INTRODUCTION

With the rapid development of semiconductor integrated circuit, the market has been increasingly competitive. Reduction of the manufacture cost becomes the key to the development of integrated circuit industry [1]. However, state-of-the-art integrated circuit design is significantly being driven toward high-density and high-complexity applications. The number of transistors in a single chip has exploded to millions, even billions. Chip area is enlarging continuously, which greatly increases the cost of chip manufacturing [2]. Therefore, seeking appropriate approaches to reduce chip area has become one of the focuses.

There are two layout area bottlenecks in integrated circuits. One is core limitation that is the internal circuit of the chip is too large to further extend. Another one is IO limitation that is significant growth in the number of IO which leads to considerable consumption of active chip area [3]. Sometimes IO area is even larger than the internal circuit area, which results in overhead of chip cost. Moreover, the growing number of IOs and layout area lead to more complex of interconnection, and affect the circuit performance [4].

For IO limitation, the unidirectional IO multiplexing circuits have been presented [5]. However, these circuits are applied in the chips which consist of several modules and these modules must have the same number of input and output. Besides, the multiplexing between input and output among different modules is not realizable. Therefore, the unidirectional IO multiplexing circuits have great limitations.

To solve the above limitations of unidirectional IO multiplexing circuits, new bidirectional IO multiplexing circuits are presented in this paper. They can be applied in the chips which consist of several modules whether these modules have the same number of input and output or not. Moreover, they realize multiplexing between input and output among different modules. As a result, new bidirectional IO multiplexing circuits increase the rate of IO multiplexing further and thus IO area and chip cost can be decreased.

IO MULTIPLEXING CIRCUITS DESIGN

New bidirectional IO multiplexing circuits are composed by distributor and multiplexer, the former makes the input signal assign to the specified module and the later picks out the output signal of specified module. The working principles and structures are introduced as following.

Working principles of IO multiplexing circuits

For the chip which consists of p modules, the structure of IO multiplexing circuit is shown as Figure 1 and $1 \le c < c+1 \le n$, $1 < e < e+1 < p$. When one of module N_1 to module N_e works, the input signal form IO is assigned to a specified module (selected from module N_1 to module N_e) according to controlling control bits M_1 to M_c. And when one of module N_{e+1} to module N_p works, the output signal of a specified module (selected from module N_{e+1} to N_p) outputs from IO according to controlling control bits M_{c+1} to M_n. It should be noted that wire W is used to prevent the multiplexer output of previous state to influence the distributor input of next state. When one of module N_1 to module N_e works, it can be realized that multiplexer output is the just data of distributor according to controlling the control bits M_{e+1} to M_n by the wire W. Therefore, the circuit can work normally.

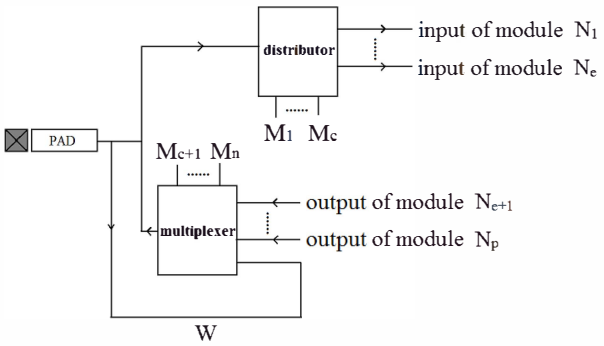

Figure 1: Structure of IO multiplexing circuit

Detail structure of IO multiplexing circuit

Tanking the chip which consists of four modules as an example, the multiplexing between the inputs of module 1 to module 3 and the output of module 4 is supposed. The detail structure of this circuit is shown as Figure 2, according to Figure 1, which includes three control bits M_1, M_2 and M_3. The Corresponding working states of control bits are shown as TABLE I, where X stands for arbitrary value. Inventor INV1 and INV2 are used to improve the drive capability of multiplexer output signal.

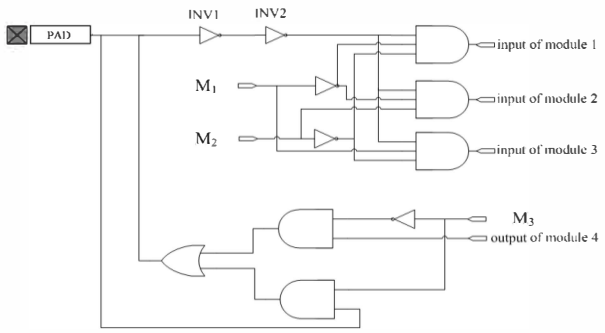

Figure 2: IO multiplexing circuit of three inputs and one output

TABLE I. CORRESPONDING WORKING STATE OF CONTROL BITS

(M_1, M_2, M_3)	**（0,0,1）**	**(0,1,1)**	**(1,0,1)**	**(X,X,0)**
Working state	Input of module 1	Input of module 2	Input of module 3	Output of module 4

ANALYSIS OF SIMULATION RESULTS

Taking the chip which consists of four modules as an example, the IO multiplexing circuits are deeply analyzed. In order to compare the circuit performance, we design IO multiplexing circuits based on static and dynamic CMOS circuit, respectively. The circuits are implemented in 0.35 μm CSMC technology. The layout area, power consumption, and delay time are simulated to obtain the high performance circuit. In order to make effective comparison, the sizes of transistors in the PUN and PDN of the two circuit structures are same.

According to Figure 2, the static and dynamic circuits are designed as Figure 3 and Figure 4, respectively. Inventor INV1 and INV2 are not shown in the Figures in order to stand out the key circuit. In the dynamic circuit, keeper transistors PM_1 to PM_4 are added to solve charge sharing problem. The simulation results of the two circuit structures are shown as TABLE II.

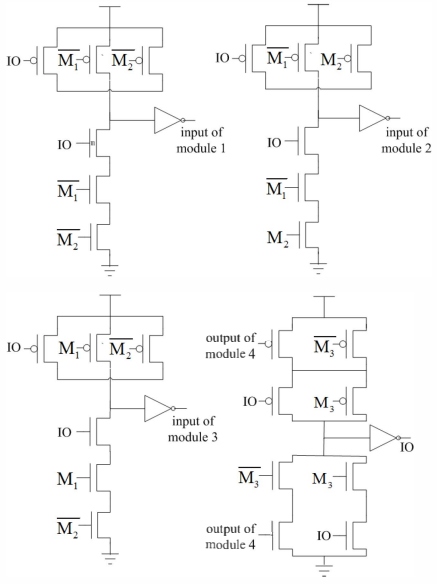

Figure 3: Static IO multiplexing circuit

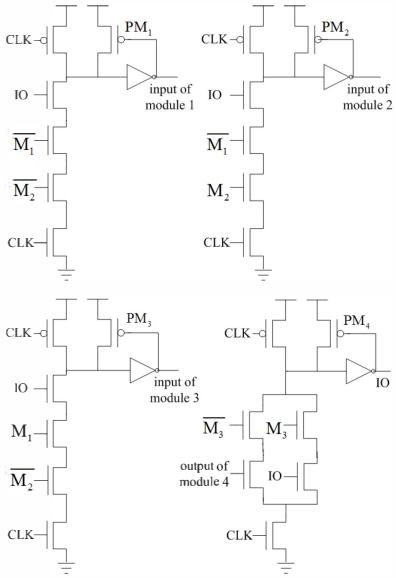

Figure 4: Dynamic IO multiplexing circuit

TABLE II. SIMULATION RESULTS OF STATIC AND DYNAMIC IO MULTIPLEXING CIRCUITS

	Working module	**Static circuit**	**Dynamic circuit**
Delay time / ns	Module 1	0.098	0.116
	Module 2	0.098	0.116
	Module 3	0.101	0.114
	Module 4	0.100	0.127
Maximum	Module 1	2.5	2

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	Working module	Static circuit	Dynamic circuit
operating frequency / Hz	Module 2	2.5	2
	Module 3	2.5	2
	Module 4	2.5	1.6
Power consumption / pw		326.8284	324.3018
PDP / pw·ns		32.4377	38.3487
Layout area / μm²		57.5×50.4	57.5×54.9

The dynamic circuits usually have shorter delay time than the static circuits due to compact PUN. But according to the simulation results, the dynamic circuit has longer delay time. This is because the PUN of static circuit is simple and the optimization of PUN in dynamic circuit is not effective. Accordingly, the two circuits have almost same charging time. However, the dynamic circuit has longer discharging time for capacitive load than the static circuit because of the additional NMOS transistor connecting CLK in the PDN. The charging and discharging time are source of delay time in CMOS circuits. So the average delay time of dynamic circuit is longer than the static circuit, and this enables the static circuit to achieve higher maximum operating frequency, as shown in TABLE II.

Besides, the size and interconnection of device influence on the power consumption greatly [6]. According to the simulation results, the power consumption of the two circuits is nearly same because of the almost same sizes and number of MOS transistors in the two circuits.

As shown in Figure 5, the left is the layout of static IO multiplexing circuit and the right is dynamic one. They are 57.5 × 50.4 μm² and 57.5 × 54.9 μm², respectively. As discussed above, the two circuits nearly have the same sizes and number of MOS transistors, so the layout area of them is almost same.

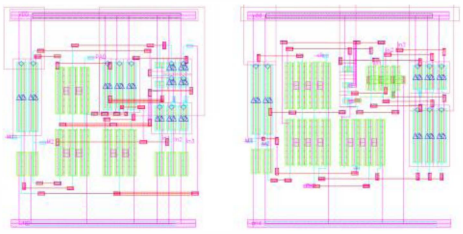

Figure 5: Layout of static and dynamic IO multiplexing circuits

Finally, as can be seen in TABLE II, the static circuit has a smaller PDP and it means the static circuit has better performance [7].

CONCLUSION

New IO multiplexing circuits are presented in this paper. It can be applied in the chips which consist of several modules whether these modules have the same number of input and output or not and realizes multiplexing between input and output among different modules. Taking the chip which consists of four modules as an example, IO multiplexing circuits based on static and dynamic CMOS circuit are designed and analyzed. The simulation results show that the maximum operating frequency and PDP of static IO multiplexing circuit are 2.5 GHz and 32.4377 pw·ns, respectively. It has higher comprehensive performance than that of its counterpart.

ACKNOWLEDGEMENTS

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