PVT VARIATIONS AWARE OPTIMAL SLEEP VECTOR DETERMINATION OF DUAL VT DOMINO OR CIRCUITS

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ABSTRACT

In this paper, determining optimal leakage vector for dual V_t domino OR circuits is explored under process, supply voltage, and temperature (PVT) variations based on 65 nm bulk and 45 nm high k/metal gate (HK+MG) technologies, while considering design parameters, environmental parameters, working characteristics of circuits, and application cases. It concludes that the high clock signal with high inputs (CHIH) vector is the optimal sleep vector for practical low leakage register files applications, and the HK+MG technology further highlights the effectiveness of the CHIH vector as compared to other vectors.

I. INTRODUCTION

As performance-critical memory components in modern processors, register files usually require a multiple read/write port capability to enable simultaneous access to execution units. This requirement, coupled with the demand for high access speed, forces the use of domino OR circuits for their local (LBL) and global bit lines (GBL) [1-2]. Specifically, sub-eight domino OR circuits (fan-in number ≤ 8) are typically utilized in practical register files due to a couple of reasons. First, eight-input domino OR circuits are typically used in LBL to achieve high performance. Secondly, if the fan-in number of GBL is high, then it is usually split into multiple GBLs to break up long RC lines.

However, as technology scales into deep nanometer regime, the domino OR circuits based bit lines leaks large current including sub-threshold leakage current (I_{sub}) and gate leakage current (I_{gate}). In addition, PVT variations, especially the within-die PVT variations induced by random variations in process and environment parameters are extremely severe in nanoscale ICs [3]. Since leakage current has a strong dependency on these parameters, PVT variations result in about 20X fluctuation in chip leakage current [3]. Therefore, reducing the leakage current of domino OR circuits is a critical issue for low power register file design.

The dual V_t technique [4] has been proved to be extremely effective in suppressing I_{sub} of wide domino OR gate by assigning low V_t transistors on the evaluation path and high V_t transistors on the precharge path. A major design concern for dual V_t wide domino OR gates is to correctly determine the proper leakage sleep vector to optimize the leakage characteristics [4]. Prior research is summarized as followed. The authors in [4] and [5] select CHIH sleep vector to achieve I_{sub} reduction. Considering the growing contribution of I_{gate}, the authors in [6] and [7] determine the high clock signal with low inputs sleep (CHIL) vector as the optimal leakage vector. Among existing studies, only [8] and [9] analyze the optimal sleep vector determination under variations. In [8], the authors propose a low clock signal and low inputs (CLIL) vector and prove that it is the optimal sleep vector under process variation. The recent work [9] presents a detailed analysis on three vectors and shows that only two vectors - CHIH and CLIL - are potential to minimize the leakage current and they have different robustness under variations: the CLIL vector is less sensitive to process variation, but the CHIH vector is more robust to temperature and supply voltage variations. However, the process variation model in [8] and [9] is not reliable to account for process variation. Also, their determination of optimal sleep vector is based on a single criterion: the robustness to variations - the ratio of mean leakage (μ) and standard deviation (σ). So, in many cases, such as ultra-low-power processors with high requirement of leakage reduction, [8] and [9] can not provide the optimal sleep vector. Hence, none of previous work is sufficient to determine the optimal sleep vector.

This paper performs a comprehensive analysis on optimal sleep vector determination for dual V_t domino OR circuits under PVT variations. The main contribution of this work is summarized as followed: (i) it re-evaluates the impact of process

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variation on optimal sleep vector determination and analyzes the influence of temperature and supply voltage variations deeply; (ii) it considers the important factors including design parameters, environmental parameters, technologies, working characteristics of circuits, and application cases while determining the optimal sleep vector.

Our analysis is based on 65 nm bulk technology (V_t of low V_t transistors: V_{tnlow} = $|V_{tplow}|$ = 0.22V; V_t of high V_t transistors: V_{tnhigh} = $|V_{tphigh}|$ = 0.35V; V_{DD} =1V) and 45 nm HK+MG technology (V_t of low V_t transistors: V_{tnlow} = 0.34 V and $|V_{tplow}|$ = 0.23V; V_t of high V_t transistors: V_{tnhigh} = 0.45 and $|V_{tphigh}|$ = 0.35V; V_{DD} =1V) [10]. All experiments are conducted by HSPICE. All domino circuits are sized to achieve 8 GHz read operation in the application of 128-entry ×32b register files.

II. IMPACT OF PROCESS VARIATION ON OPTIMAL SLEEP VECTOR DETERMINATION

Variations in important process parameters including random discrete doping (N_{ch}), gate length (L_{eff}), and gate oxide thickness (t_{ox}) influence the leakage current characteristics of dual V_t domino OR circuits significantly. In this section, the impact of process variation on optimal sleep vector determination is discussed.

A. Inaccuracy of 10%PP Model

Table I compares the process model (10%PP) in prior work and process variation specified by latest International Technology Roadmap for Semiconductors (ITRS) [11]. Since I_{sub} and I_{gate} strongly dependent on these process parameters, 10%PP model leads to an inaccurate estimation of leakage current variation. Fig. 1 shows the leakage current variation of minimum sized NMOS devices at room temperature in 65 nm bulk and 45 nm HK+MG technologies, which shows that 10%PP model results in significant underestimation in I_{sub} variation and a small overestimation in I_{gate} variation. Therefore, 10%PP is not reliable enough to characterize the impact of process variation.

Note that, 45 nm HK+MG technology introduces extra V_t variability due to the interface roughness. Thus, it generates larger I_{sub} variation. But at the same time, the HK+MG technology decreases I_{gate} variation effectively since I_{gate} variation is directly proportional to exp(-K) [12]. So, the relative contribution of I_{sub} variation is larger for 45 nm HK+MG technology and accordingly, the underestimation of I_{sub} variation caused by 10%PP model is more significant, as shown in Fig. 1.

Since I_{sub} dominates the leakage current with the CLIL vector and I_{gate} dominates the leakage current with the CHIH vector in dual V_t domino OR circuits [9], the robustness of the CHIH and CLIL vectors against process variation are also respectively underrated and overrated in prior work. Therefore, there is a need to re-evaluate the influence of process variation on optimal sleep vector determination in dual V_t domino OR circuits.

Table 1: Comparison of process parameter models

%10PP [8-9]	Process	L_{eff}	t_{ox}	N_{ch}
	3σ	10%	10%	10%
Latest ITRS	Process	L_{eff}	t_{ox}	V_t [1]
	3σ	12%	5%	40%

[1] doping variability induced V_t variation

B. Re-evaluation of process variation impact

As also observed in Fig. 1, in the presence of process variation, I_{sub} variation is much larger than I_{gate} variation for the same device (~7X for 65 nm and ~58X for 45 nm technologies), so I_{sub} variation dominates the total leakage current variation. In this subsection, we first discuss I_{sub} variation with two potential sleep vectors based on analytical formulas. Then, we re-evaluate the robustness of two sleep vectors to process variation.

I_{sub} of a N-input domino OR circuit with two potential sleep vectors can be expressed as [9]:

$$\begin{cases} I_{sub}^{CHIH} = \sum_i [W_{HN}]_i \cdot J_{SHN} + \sum_j [W_{HP}]_j \cdot J_{SHP} = \alpha_1 \cdot J_{SHN} + \alpha_2 \cdot J_{SHP} \\ I_{sub}^{CLIL} = \sum_k [W_{LP}]_k \cdot J_{SLP} = \alpha_3 \cdot J_{SLP} + \eta \cdot \alpha_4 \cdot J_{SLN} \end{cases} \quad (1)$$

where J_{SHN}, J_{SHP}, J_{SLN}, and J_{SHP} are I_{sub} density per width unit of high V_t NMOS, high V_t PMOS, low V_t NMOS, and low V_t PMOS, respectively. η is given as

$$\eta = (N \cdot \alpha_5)^{\frac{\lambda_{DIBL}}{1+2\lambda_{DIBL}}} \cdot 10^{\frac{-\lambda_{DIBL} V_{dd}}{S}\left(\frac{1+\lambda_{DIBL}}{1+2\lambda_{DIBL}}\right)} \quad (2)$$

where λ_{DIBL} is the drain induced barrier lowering (DIBL) factor; S is the sub-threshold swing; α_1-α_2 only depend on the gate width of devices. Since gate width of devices in dual V_t domino OR circuits is usually much larger than L_{eff}, gate width variation can be neglected and α_1-α_2 remain constant. However, both of DIBL effect and S are PVT dependent and thus η variation is induced by PVT variations. Accordingly, I_{sub} variation with two sleep vectors can be expressed as:

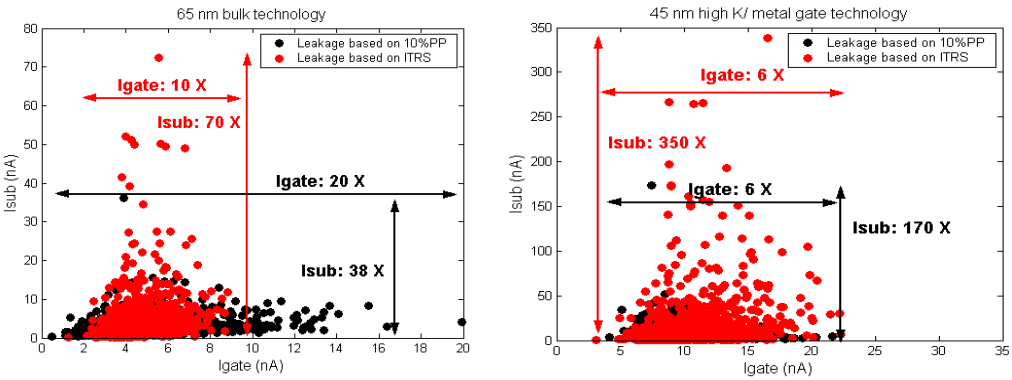
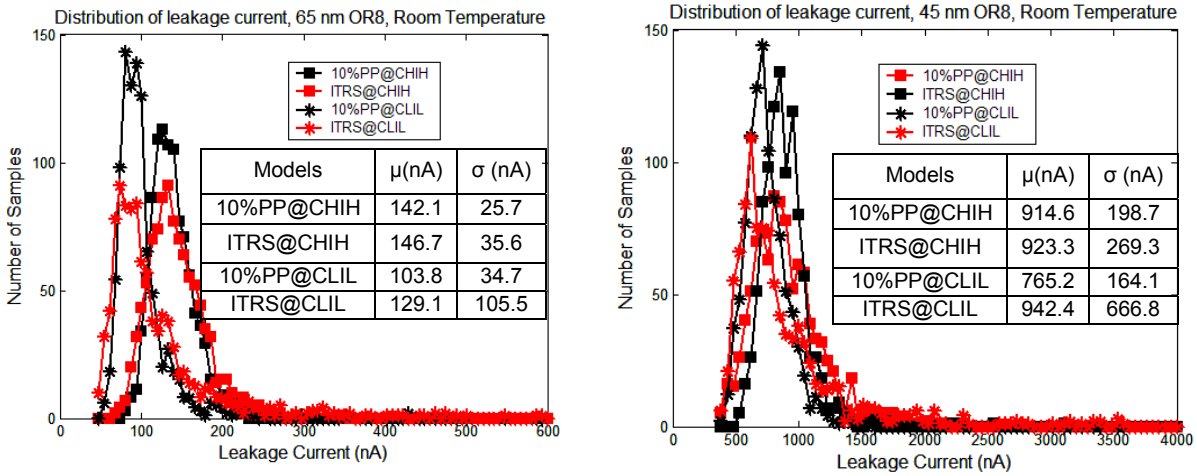


Figure 1: Scatter plots for leakage current of NMOS devices obtained with minimum size using Monte Carlo simulations.



Models	μ(nA)	σ (nA)
10%PP@CHIH	142.1	25.7
ITRS@CHIH	146.7	35.6
10%PP@CLIL	103.8	34.7
ITRS@CLIL	129.1	105.5

Models	μ(nA)	σ (nA)
10%PP@CHIH	914.6	198.7
ITRS@CHIH	923.3	269.3
10%PP@CLIL	765.2	164.1
ITRS@CLIL	942.4	666.8

Figure 2: Distribution of leakage current in dual V_t domino OR8 circuits

$$\begin{cases} \dfrac{\partial I_{sub}^{CHIH}}{\partial(P,V,T)} = \alpha_1 \cdot \dfrac{\partial J_{SHN}}{\partial(P,V,T)} + \alpha_2 \cdot \dfrac{\partial J_{SHN}}{\partial(P,V,T)} \\ \dfrac{\partial I_{sub}^{CLIL}}{\partial(P,V,T)} = \alpha_3 \cdot \dfrac{\partial J_{SLP}}{\partial(P,V,T)} + \eta \cdot \alpha_4 \cdot \dfrac{\partial J_{SLN}}{\partial(P,V,T)} + \alpha_4 \cdot J_{SLN} \cdot \dfrac{\partial \eta}{\partial(P,V,T)} \end{cases} \quad (3)$$

We can see that I_{sub} variation with the CHIH vector depends on I_{sub} variation in high V_t transistors, but I_{sub} variation with the CLIL vector depends on I_{sub} variation in low V_t devices. Since the effect of process variations on I_{sub} is substantially smaller for high V_t transistors and also I_{sub} variation with the CHIH vector does not depend on the fan-in number N, CHIH vector leads to a smaller I_{sub} variation and further a smaller total leakage variation as compared to the CLIL vector. Fig. 2 shows leakage current distribution of dual V_t domino OR8 circuits obtained from Monte Carlo simulations of 1000 samples, which shows the better robustness (large μ/σ) of CHIH vector to process variation. Another important observation is that the underestimation of 10%PP model-based analysis is more pronounced for 45 nm HK+MG technology.

III. IMPACT OF SUPPLY VOLTAGE AND TEMPERATURE VARIATIONS

In addition to process variation, changes in operating conditions including temperature and supply voltage also significantly impact the determination of optimal sleep vector in dual V_t domino OR circuits. The work [9] concludes that the CHIH vector is more robust to temperature and supply voltage variations, but it fails to provide detailed analysis. In this section, the impact of temperature and supply voltage variations is investigated deeply.

A. Impact of Temperature Variation

In MOS devices, I_{sub} has stronger temperature dependency than I_{gate}. Since I_{gate} dominates the leakage current with the CHIH vector, the CHIH vector is more robust to temperature variation.

B. Impact of Supply Voltage Variation

Both I_{gate} and I_{sub} of MOS devices have exponential dependencies on V_{dd}, but I_{gate} depends on V_{dd} more strongly. Therefore, I_{gate} is more sensitive to supply voltage variation which significantly affects the total leakage variation. In this subsection, I_{gate} variation with two sleep vectors under supply voltage variation is discussed analytically and then the robustness of two potential optimal sleep vectors is discussed.

I_{gate} in dual V_t domino OR circuits with two sleep vectors can be expressed as [9]

$$\begin{cases} I_{gate}^{CHIH} = \sum_i [W_{LN}]_i \cdot J_{GFLN} + \frac{1}{2} \cdot \sum_j [W_{HN}]_j \cdot J_{GRHN} \cong N \cdot W_{LN}^{PDN} \cdot J_{GFLN} \\ I_{gate}^{CLIL} = \frac{N}{2} \cdot W_{LN}^{PDN} \cdot J_{GRLN} + \sum_k [W_{HN}]_k \cdot J_{GFHN} \cong \frac{1}{2} N \cdot W_{LN}^{PDN} \cdot J_{GRLN} \end{cases} \quad (4)$$

where J_{GFLN} and J_{GFHN} are forward I_{gate} density per unit width of low V_t and high V_t NMOS, respectively; J_{GRLN} and J_{GRHN} are reverse I_{gate} per unit width of low V_t and high V_t NMOS, respectively; W_{LN}^{PDN} is the gate width of low V_t devices in PDN and it is a constant under PVT variations.

Therefore, I_{gate} variation can be written as

$$\begin{cases} \frac{\partial I_{gate}^{CHIH}}{\partial(P,V,T)} \cong N \cdot W_{LN}^{PDN} \cdot \frac{\partial J_{GFLN}}{\partial(P,V,T)} \\ \frac{\partial I_{gate}^{CLIL}}{\partial(P,V,T)} \cong \frac{1}{2} N \cdot W_{LN}^{PDN} \cdot \frac{\partial J_{GRLN}}{\partial(P,V,T)} \end{cases} \quad (5)$$

Based on the above analysis, we can see that I_{gate} in dual V_t domino OR circuits is mainly generated by low V_t devices in PDN and footer, which can be called I_{gate}-generating-network (GGN). Also, as verified in our simulation, due to the similar mechanism, J_{GF} and J_{GR} have similar dependencies on V_{dd}. Therefore, if GGN is under the same supply voltage variation, based on (5), I_{gate} variation with the CHIH sleep vector is about twice as large as that with the CLIL sleep vector.

However, in practice, the influences of supply variation on GGN are different. In a domino OR gate with the CHIH vector, the pre-charger and keeper are both OFF and the dynamic node is isolated from supply voltage variation. So the voltage of dynamic node stays almost zero (see Fig. 3) and therefore I_{gate} variation is reduced effectively. Alternatively, with the CLIL vector, the pre-charger and keeper are both ON. If supply voltage varies, the voltage at the dynamic node is also changed by the same amount (see Fig. 3). So supply voltage variation is introduced to GGN directly, thereby producing larger I_{gate} variation.

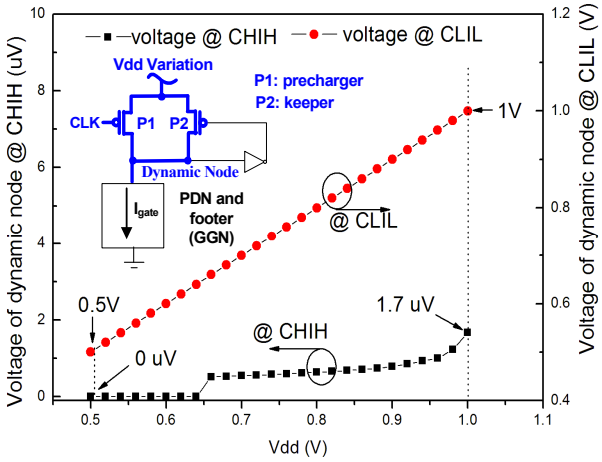


Figure 3: Voltage variation of dynamic node in 65 nm OR8 gate

Hence, the CHIH vector is more robust to supply voltage variation.

To this point, we have investigated the robustness of two sleep vectors to PVT variations and concluded that CHIH vector is more robust to PVT variations as compared to its counterpart CLIL vector. In the following section, we will take into account the effectiveness of two sleep vectors and provide a comprehensive study of optimal sleep vector determination in different application cases.

IV. PVT VARIATIONS AWARE OPTIMAL SLEEP VECTOR DETERMINATION

Our analysis adopts process variation specified by the latest ITRS in Table I. As also reported by the latest ITRS, the supply voltage is assumed to have an independent normal Gaussian distribution with 3σ variation of 10%. Since temperature variation in practical sleep circuits depends on the interval of sleep mode, our analysis considers two types of sleep circuits: (1) circuits with short standby intervals (SSI). During short sleep period, the sleep temperature of circuits changes from typical working temperature 110°C to room temperature; (2) circuits with long standby intervals (LSI). The sleep temperature can be assumed to stay at room temperature with only 1°C variation. 1000 Monte Carlo simulations are done to achieve enough statistical accuracy.

Considering the requirement for leakage reduction and robustness to variations in different application cases, we define Leakage-Variation-Cost (LVC) as

$$LVC=\lambda\mu+(1-\lambda)(\sigma/\mu) \quad (7)$$

where μ is used to evaluate the leakage reduction; σ/μ is the uncertainty of leakage current; λ is the weighting factor, which indicates the relative significance of leakage reduction and robustness in different application cases. Clearly, λ is a real number and $\lambda \in [0, 1]$. Obviously, the sleep vector with minimum LVC value with different λ corresponds to the optimal sleep vector in different application cases.

Fig.4 compares LVC of three sleep vectors for different dual V_t domino OR circuits in two technologies. First, we can see that for all circuits, the CHIL vector results in maximum LVC in all application cases. For two potential optimal sleep vectors CHIH and CLIL, their LVC comparison changes with the fan-in number of circuits. Take 65 nm circuits as an example: for OR2 circuits, as compared to the CLIL vector, the achieved LVC savings with the CHIH vector ranges from 41.7% to 75.2% for LSI and from 58.4% to 88.5% for SSI; for OR8 circuits, LVC with the CHIH vector is still the minimum in all cases, but it is very close to that with the CLIL vector; as the fan-in number is increased to 32, LVC with the CHIH vector is smaller than CLIL only in the extreme case with $\lambda<0.01$, when the robustness is the top design priority. The main reason is that, with the increasing of N, the number of parallel paths in GGN becomes larger and so I_{gate} increases accordingly, as expressed in Equation (5). Therefore, the CLIL vector, which minimizes I_{gate}, can achieve minimum average leakage current. It is important to note that, for sub-eight input OR circuits in two technologies, the CHIH vector is able to achieve the minimum LVC in all application cases. Furthermore, as evident from Fig. 4, due to the smaller temperature variation for LSI, LVC of SSI is always larger than that of SSI in the same application.

We further compare different sleep vectors based on three general cost criteria under variations: $C_1=0.5\mu+0.5\sigma$, which shows the variation cost in typical case; $C_2=\mu+6\sigma$, which indicates the variation cost in worst case; $C_3=\mu\times\sigma$, which evaluates the overall cost under variations.

Table V lists the comparison result based on three general criteria. Similar to LVC-based comparison in Fig. 4, the CHIL vector is the worst vector under PVT variations; the CLIL vector is more likely to become the optimal sleep vector for wide dual V_t domino OR circuits; but CHIH is still the optimal sleep vector for sub-eight dual V_t domino OR circuits in all cases.

From the above discussion, we can see that the optimal sleep vector determination for dual V_t domino OR circuits is a complex issue and it depends on multiple factors. However, the CHIH vector is the optimal sleep vector for sub-eight dual V_t domino OR circuits, which is the typical application in practical register files. PVT variations, as we demonstrate, can significantly alter our gating decisions in dual V_t domino OR circuits.

IV. CONCLUSION

This paper, for the first time, focuses on determining optimal sleep vector for dual V_t domino OR circuits under PVT variations and performs a comprehensive analysis based on latest ITRS projection, while considering important factors including design parameters, environmental parameters, technologies, working characteristics of circuits, and application cases. Our analysis shows that the CHIH vector is the optimal sleep vector for practical low leakage register file applications.

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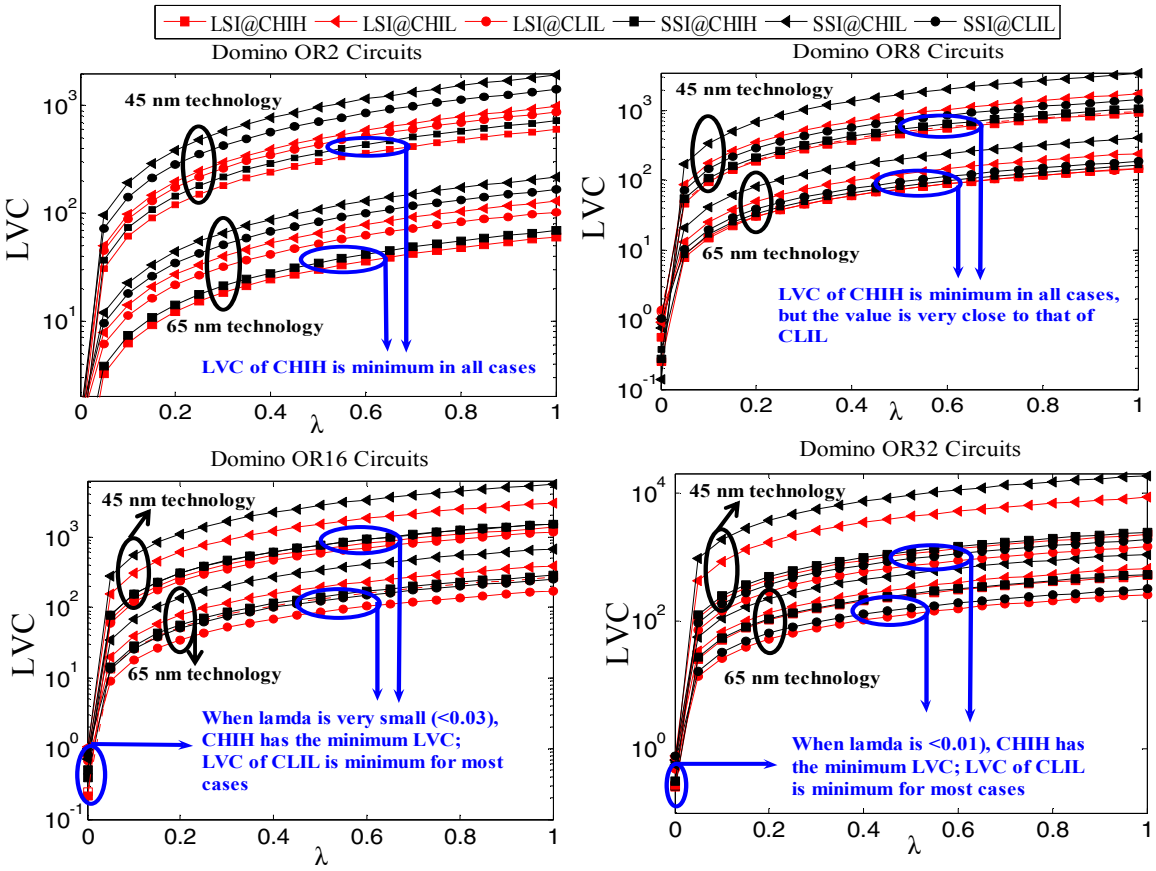

Figure 4: LVC of dual V_t domino OR circuits with different sleep vectors

Table 2 Three criteria based comparison of leakage current in dual V_t domino OR circuits

Cost	Vector	T	65nm bulk technology					45nm HK+MG technology				
			OR2	OR4	OR8	OR16	OR32	OR2	OR4	OR8	OR16	OR32
C_1	CHIH	LSI/ SSI	38/ 48	56/ 74	92/ 112	164/ 195	316/ 334	506/ 542	516/ 598	727/ 770	819/ 1147	1404/ 1592
	CHIL	LSI/ SSI	148/ 232	232/ 241	249/ 355	338/ 583	553/ 926	890/ 1956	1290/ 2280	1660/ 1941	3118/ 5507	7570/ 14430
	CLIL	LSI/ SSI	106/ 196	182/ 151	175/ 180	143/ 241	191/ 255	773/ 1492	797/ 1331	866/ 1457	1070/ 1387	1248/ 1643
C_2[1]	CHIH	LSI/ SSI	0.16/ 0.22	0.22/ 0.38	0.37/ 0.53	0.65/ 0.93	1.27/ 1.36	0.30/ 0.29	0.26/ 0.30	0.41/ 0.39	0.31/ 0.61	0.58/ 0.70
	CHIL	LSI/ SSI	1.13/ 1.70	1.89/ 1.54	1.77/ 2.25	2.13/ 3.62	3.33/ 5.60	0.58/ 1.39	0.91/ 1.54	1.12/ 0.62	2.23/ 3.85	4.83/ 8.07
	CLIL	LSI/ SSI	0.75/ 1.52	1.55/ 0.98	1.37/ 1.21	0.86/ 1.66	1.00/ 1.48	0.49/ 1.08	0.50/ 0.91	0.55/ 1.03	0.70/ 0.90	0.78/ 1.05
C_3[2]	CHIH	LSI/ SSI	0.09/ 0.18	0.20/ 0.47	0.54/ 0.98	1.70/ 3.05	6.46/ 7.34	0.25/ 0.26	0.23/ 0.30	0.49/ 0.50	0.38/ 1.17	1.32/ 1.84
	CHIL	LSI SSI	2.17/ 5.33	5.10/ 5.73	6.21/ 12.3	11.2/ 33.1	29.4/ 82.7	0.78/ 3.82	1.66/ 5.18	2.75/ 1.60	9.71/ 30.3	56.4/ 192
	CLIL	LSI SSI	1.11/ 3.75	2.98/ 2.25	2.99/ 3.22	1.96/ 5.81	3.20/ 6.11	0.59/ 2.22	0.62/ 1.77	0.74/ 2.12	1.14/ 1.90	1.52/ 2.66

[1] The unit is 10^3 for 65 nm and 10^4 for 45 nm technology [2] The unit is 10^4 for 65 nm and 10^5 for 45 nm technology