Optimization and Predication of Leakage Current Characteristics in Wide Domino OR Gates Under PVT Variation

Na Gong and Ramalingam Sridhar
University at Buffalo, State University of New York, Buffalo, NY 14260-2000
{nagong,rsridhar}@buffalo.edu

ABSTRACT

The leakage current characteristics of wide dual V_t domino OR gates is studied and gate-level models for estimating sub-threshold leakage and gate leakage current with two different sleep states are developed to determine the optimal sleep state. Results demonstrate that the developed models are robust and exhibit maximum error of 4% with respect to device-level BSIM4 models based HSPICE simulations. Furthermore, PVT variation aware leakage current characteristics of domino OR gates is analyzed and the optimal sleep state is obtained.

I. INTRODUCTION

As one of the most critical building blocks, wide domino OR circuits or similar structures are extensively employed in register and cache array bit lines to achieve simple and fast design [1]. However, along with the progress of advanced VLSI technology, the reduction of the threshold voltage (V_t) and gate oxide thickness (t_{ox}) leads to the exponential increase in the sub-threshold leakage current (I_{sub}) and gate leakage current (I_{gate}), which has become an imperative design challenge. Also, for wide domino OR gates which refer to N-input structure when N>4, the parallel evaluation transistors in Pull down network (PDN) are prone to leaking charge from the evaluation node. This further highlights the importance of leakage current reduction.

The dual V_t technique proposed in [2] has been proved to be extremely effective in suppressing I_{sub} of wide domino OR gate by assigning low V_t devices in the evaluation path and high V_t devices in the precharge path of the circuits. A major design challenge when applying dual V_t technique is to obtain the optimal sleep state to minimize the leakage current, which would greatly affect the effectiveness for leakage reduction [2]. Several attempts have been made to address this issue in the literature. These papers can be divided into two groups: designers in the first category try to set a high clock signal with high inputs (CHIH) state in sleep period to achieve low leakage design [2-3]. However, this state focuses only on I_{sub}. On the other hand, papers in the second group adopt the high clock signal with low inputs sleep state (CHIL) as the lowest leakage state [4-5], but this state neglects large I_{gate} produced by the footer. Our recent work [6] proposed CLIL (the clock signal and inputs are all low) state and it has indicated that only the CHIH and CLIL states are potential to improve the leakage current of domino circuits: CHIH is effective to suppress the leakage current of low fan-in domino circuits at high temperature and CLIL state is preferable to reduce the leakage current of wide domino circuits at high temperature and most of domino circuits at room temperature.

However, no existing work provides accurate models of leakage current in wide domino OR gates with different sleep states. So designers could only rely on SPICE simulation to obtain leakage current with different sleep states and then compare simulation results to determine the optimal state. To obtain I_{sub} and I_{gate} of an OR gate in simulation, however, designers need to modify parameters in netlists and perform simulations repeatly. More importantly, accurate models can help designers understand the sleep state dependent leakage current characteristics thoroughly and continue future research, such as low leakage gate. To make things worse, the increasing variations in process, supply voltage, and temperature (PVT) with continuously device dimension shrinking have a significant impact on leakage current characteristics [7]. But only [6] considered the influence of process variation and all of these existing studies fail to account for combined PVT variation. Thus, they are not robust enough to solve the optimal sleep state issue in wide domino OR gates. As a significant extension, this paper aims (1) to develop gate-level accurate models of I_{sub} and I_{gate} to characterize the leakage current in wide domino OR gates; (2) to investigate leakage current characteristics of wide domino OR gates under PVT variation and obtain the optimal sleep state in such variation environment.

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II. BASIS OF LEAKAGE CURRENT ANALYSIS

The leakage current analysis in this paper is based on device-level BSIM4 models [7], which include I_{sub} and I_{gate} in transistors. BSIM4 models are used in this paper in 65nm (V_{tnlow} = $|V_{tplow}|$ = 0.22V, V_{tnhigh} = $|V_{tphigh}|$ = 0.35V, and V_{DD} =0.8V) and 45nm CMOS technologies (V_{tnlow} = $|V_{tplow}|$ = 0.22V, V_{tnhigh} = $|V_{tphigh}|$ = 0.35V, and V_{DD} =1.0V).

During the analysis, this paper adopts "Dividing Two Parts" (DTP) principle, which separates domino circuit into two parts: (I) low V_t NMOS transistors in PDN and footer (II) the rest circuit including high V_t PMOS pre-charge transistor P1 and keeper P2, and two inverters. For domino circuits with various functions and fan-in numbers, Part II always stays the same and only Part I varies accordingly. Therefore, for either sleep state, the contribution of Part II to a specific leakage current will not change and DTP simplifies the analysis.

Also, this paper examines leakage current characteristics of domino wide OR gates at upper and lower sleep temperature extremes of high performance microprocessor dies. The sleep temperature 110°C assumes that the sleep period is very short and the sleep temperature keeps at active temperature 110°C. Alternatively, the sleep temperature 25°C indicates that the sleep temperature has fallen to the room temperature in long sleep period.

For convenience, different leakage current components in this paper are represented by capital letters in subscript: G: I_{gate}, S: I_{sub}, F: forward I_{gate}, R: reverse I_{gate}, L: low V_t device, H: High V_t device, N: NMOS and P: PMOS. For example, I_{GRLN} denotes reverse I_{gate} of low V_t NMOS and I_{SHP} denotes I_{sub} of high V_t PMOS.

Fig. 1 shows paths of I_{gate} and I_{sub} in wide domino OR gates with two sleep states, which will be discussed in the following sections.

III. I_{GATE} IN WIDE DOMINO OR GATES

Based on device-level BSIM4 models, in this section, gate-level models for I_{gate} in wide domino OR gates with different sleep states are developed.

A. I_{gate} of MOS devices

Gate leakage components produced by MOS devices depends on bias conditions. Both ON and OFF transistors produce I_{gate}. In an "on" MOS transistor, forward I_{gate} (I_{GF}) mainly consists of gate-to-channel tunneling currents (I_{gcs} and I_{gcd}), which flows from gate to source/drain through channel. Alternately, in an OFF MOS device, reverse I_{gate} (I_{GR}) is mainly composed of edge-direct-tunneling (EDT) currents (I_{gso} and I_{gdo}), which flows from source/drain to gate through source-drain extension [8]. Based on BSIM4 model, I_{gate} per unit width adopts a common expression for different components [8]:

$$J_G = A \cdot L \cdot \left(\frac{T_{oxref}}{t_{ox}}\right)^{ntox} \cdot \frac{V_g \cdot V_{aux}}{t_{ox}^2} \cdot e^{-B\left(\alpha - \beta\left|V_{ox}\right|\right)\left(1+\gamma\left|V_{ox}\right|\right)\cdot t_{ox}} \quad (1)$$

where A and B are physical parameters and their values are given by [7], α, β, γ and ntox are parameters provided in BSIM4 models. V_{aux} denotes the voltage across the oxide and it has different expressions for each component according to [8].

Fig. 2 (a) and (b) shows 65nm and 45nm BSIM4 models based HSPICE simulation results of I_{gate} in MOS devices. As expected, I_{gate} of PMOS is one order less than that of NMOS. More importantly, I_{GF} is larger than I_{GR} 56% and 51% for low V_t NMOS transistors in 65nm and 45nm technologies, respectively. As also observed in Fig. 2, I_{gate} is almost insensitive to temperature.

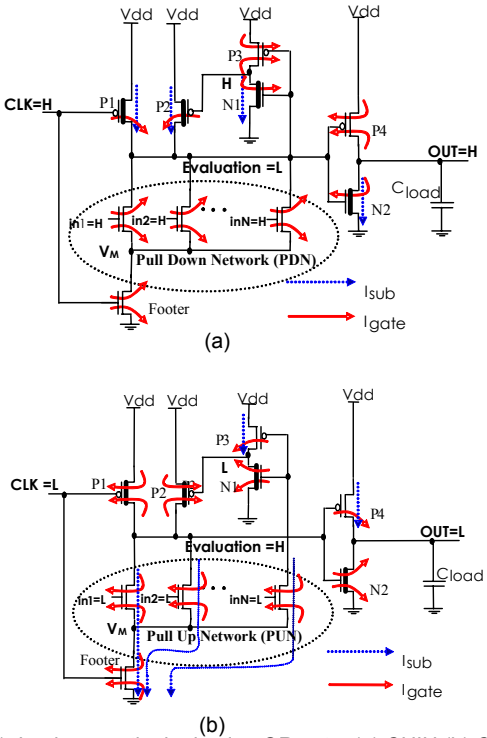
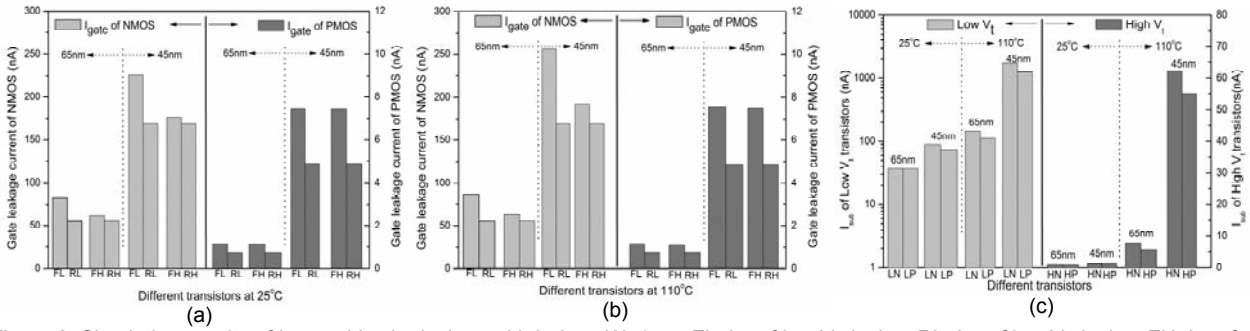


Figure 1: Leakage paths in domino OR gate. (a) CHIH (b) CLIL. Devices with bold lines represent high V_t transistors.



(a) (b) (c)

Figure 2: Simulation results of I_{gate} and I_{sub} in devices with L=L_{min}, W=1μm. FL: I_{GF} of low V_t device, RL: I_{GR} of low V_t device, FH: I_{GF} of high V_t device, RH: I_{GR} of high V_t device, LN: Low V_t NMOS LP: Low V_t NMOS PMOS HN: High V_t N: NMOS HP: High V_t PMOS

B. Modeling of I_{gate} of wide domino OR gates with CHIH state

Based on DTP principle, I_{gate} of N-input domino OR gate with CHIH can be expressed as

$$I_{gateCHIH}=\sum_i I_{gatei}=I_{gateI}+I_{gateII} \quad (2)$$

Ignoring the voltage drop across the ON NMOS transistors in PDN, the expression of I_{gateI} is

$$I_{gateI}=(N+1)\times W_{LN}\cdot J_{GFLN}=(N+1)\times I_{GFLN} \quad (3)$$

Assuming the NMOS transistors in PDN and footer have the same size, then (3) can be rewritten as

$$I_{gateI}=I_{gatePDN}+I_{gateFooter}=\left(NW_{PDN}+W_{Footer}\right)\cdot J_{GFLN} \quad (4)$$

And I_{gateII} can be modeled as

$$I_{gateII}=\sum_{i=1}^{4} I_{P_i}+\sum_{j=1}^{2} I_{N_j} \quad (5)$$

Based on the analysis of Section III-A, I_{gate} of PMOS can be negligible as compared to that of NMOS, so

$$I_{gateII}=\sum_{j=1}^{2} I_{N_j}=\left(W_{N1}+W_{N2}\right)\cdot J_{gdoHN}=\frac{W_{N1}+W_{N2}}{2}\times I_{GRHN} \quad (6)$$

If $W_{N1}=W_{N2}=W_{HN}$, one arrives at

$$I_{gateII}=W_{HN}\cdot J_{GRHN}=I_{GRHN} \quad (7)$$

Thus $I_{gateCHIH}=(N+1)\times I_{GFLN}+I_{GRHN}$ (8)

Observe that I_{gate} of wide OR gates with CHIH state is mainly composed of I_{GF} generated by PDN and footer. Also, without considering voltage drop in this analysis can result in over-estimate, as will be revealed in the experiments.

C. Modeling of I_{gate} of wide domino OR gates with CLIL state

As shown in Fig. 1 (b), I_{gateI} and I_{gateII} are modeled as followed.

$$I_{gateI}=I_{gatePDN}+W_{Footer}\cdot J_{gdoRLN} \quad (9)$$

$$I_{gatePDN}=N\cdot W_{PDN}\cdot\left(J_{gsoLN}+J_{gdoLN}\right) \quad (10)$$

At CLIL state, $|V_{gs1}|=|V_{gd2}|=|V_M|$ and $|V_{gd1}|=V_{dd}$ (11)

where V_{gs1} and V_{gd1} are V_{gs} and V_{ds} of transistors in PDN, V_{gd2} is V_{gd} of footer. V_M represents intermediate node voltage between PDN and footer, as shown in Fig. 1. Note that V_M is very small compared to V_{dd} [9]. Therefore, the dominant contributor of $I_{gatePDN}$ is J_{gdoLN} and I_{gdo} produced by footer can be neglectable. So (9) becomes

$$I_{gateI}=\frac{N}{2}\cdot W_{PDN}J_{GRLN}=\frac{N}{2}\cdot I_{GRLN} \quad (12)$$

Similarly, I_{gate} of PMOS in Part II can be negligible, so

$$I_{gateII}=\sum_{j=1}^{2} I_{N_j}=\left(W_{N1}+W_{N2}\right)\cdot J_{GFHN} \quad (13)$$

Assuming $W_{N1}=W_{N2}=W_{HN}$,

$$I_{gateII}=2W_{HN}\cdot J_{GFHN}=2I_{GFHN} \quad (14)$$

Therefore, I_{gate} of wide OR gates with CLIL can be modeled as

$$I_{gateCLIL}=2I_{GFHN}+\frac{\mathrm{N}}{2}\cdot I_{GRLN} \quad (15)$$

Note that I_{gate} of wide domino OR gates with CLIL state mainly consists of I_{GR} produced by low V_t NMOS transistors in PDN and footer. As discussed in Section III-A, I_{GR} is less than I_{GF} greatly and therefore CLIL state minimizes I_{gate} of wide OR gates. Also, ignoring the contribution of PMOS to I_{gate} can lead to under-estimate, which will be discussed later.

IV. I_{SUB} IN WIDE DOMINO OR GATES

This section develops models for I_{sub} in wide domino OR gates with different sleep states.

A. I_{sub} of MOS devices

I_{sub} is the diffusion current flowing between source and drain when a MOS device is turned off ($V_{gs}<V_{th}$). According to BSIM4 model [8], I_{sub} per unit width can be modeled as

$$J_s=\frac{1}{L_i}I_0\exp\left(\frac{V_{gs}-V_{th}-V_{off}^{'}}{nKT/q}\right)\left(1-\exp\left(-\frac{V_{ds}}{KT/q}\right)\right) \quad (16)$$

For OFF MOS devices in nanoscale domino OR gates. V_{ds} is relatively much larger than KT/q, so (16) can be simplified to

$$J_S = \frac{1}{L} I_0 \exp\left(\frac{V_{gs} - V_{th} - V'_{off}}{nKT/q}\right) \quad (17)$$

Fig. 2 (c) shows HSPICE simulation results of I_{sub} in MOS devices. As expected, high V_t transistors produce much less than that of low V_t transistors. Also, due to the reduction in V_t and increase in thermal voltage, I_{sub} has stronger dependence on temperature compared to I_{gate} (See Fig. 2 (a) and (b)).

A. Modeling of I_{sub} of wide domino OR gates with CHIH state

As shown in Fig. 1(a), low V_t transistors are all turned on with CHIH state and therefore I_{sub} is only produced by OFF high V_t transistors in Part I of the circuit. So

$$I_{subCHIH} = I_{subI} = \sum_i I_{subi} = (W_{P1} + W_{P2}) \cdot J_{SHP} + (W_{N1} + W_{N2}) \cdot J_{SHN} \quad (18)$$

Ideally, the V_{gs} of these transistors are all about zero, so I_{sub} can be expressed as

$$I_{subCHIH} = (W_{P1} + W_{P2}) \cdot \frac{1}{L} I_0 \exp\left(\frac{-V_{thHP} - V'_{off}}{nKT/q}\right) + (W_{N1} + W_{N2}) \cdot \frac{1}{L} I_0 \exp\left(\frac{-V_{thHN} - V'_{off}}{nKT/q}\right) \quad (19)$$

To simplify (19), we assume $W_{P1} = W_{P2} = W_{HP}$ and $W_{N1} = W_{N2} = W_{HN}$, so I_{sub} can be expressed as:

$$I_{subCHIH} = 2W_{HP} \cdot J_{SHP} + 2W_{HN} \cdot J_{SHN} = 2(I_{SHP} + I_{SHN}) = \frac{2I_0}{L} \cdot \left(W_{HP} \exp\left(\frac{-V_{thHP} - V'_{off}}{nKT/q}\right) + W_{HN} \exp\left(\frac{-V_{thHN} - V'_{off}}{nKT/q}\right) \right) \quad (20)$$

Therefore, CHIH state can suppress I_{sub} effectively for a couple of reasons. First, I_{sub} with CHIH state is produced by all high V_t transistors, which is much less than low V_t transistors. Second, I_{sub} of N-input OR gate with CHIH state is a constant with N.

B. Modeling of I_{sub} of wide domino OR gates with CLIL state

Unlike I_{sub} with CHIH state, I_{sub} with CLIL is produced by transistors in two parts of wide OR gates. In Part I, the PDN and footer are all turned off. Thus, it can be modeled as a stack of two transistors, as shown in Fig. 3. Based on I_{sub} model of a stack of two off transistors in [10],

$$I_{subI} = I_{subStack} = W_u^{\alpha} W_{Footer}^{1-\alpha} 10^{\frac{-\lambda_d V_{dd}}{S}(1-\alpha)} \cdot J_{SLN} \quad (21)$$

where $\alpha \approx \frac{\lambda_d}{1+2\lambda_d}$, S is the sub-threshold swing and λ_d is the drain-induced barrier lowering (DIBL) factor.

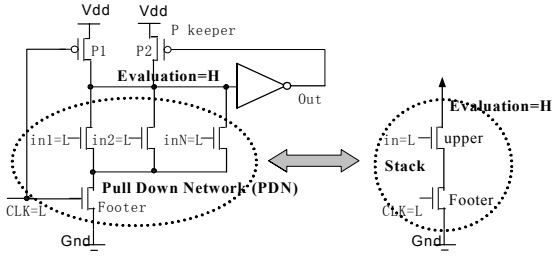


Figure 3: Model of PDN and footer

Note that $W_u = N \cdot W_{LN}$ when the transistors in parallel have the same size and (21) becomes

$$I_{subI} = N^{\alpha} \cdot 10^{\frac{-\lambda_d V_{dd}}{S}(1-\alpha)} \cdot W_{LN} \cdot J_{SLN} = K \cdot I_{SLN} = K \cdot W_{LN} \cdot \frac{I_0}{L} \cdot \exp\left(\frac{-V_{thLN} - V'_{off}}{nKT/q}\right) \quad (22)$$

where $K = N^{\frac{\lambda_d}{1+2\lambda_d}} \cdot 10^{\frac{-\lambda_d V_{dd}}{S}\left(\frac{1+\lambda_d}{1+2\lambda_d}\right)}$ (23)

$$I_{subII} = (W_{P3} + W_{P4}) \cdot J_{SLP} \quad (24)$$

Assuming $W_{P3} = W_{P4}$

$$I_{subII} = 2W_{LP} \cdot J_{SLP} = 2W_{LP} \cdot \frac{I_0}{L} \cdot \exp\left(\frac{-V_{thLP} - V'_{off}}{nKT/q}\right) \quad (25)$$

So, I_{sub} with CLIL state can be determined by the model

$$I_{subCLIL} = 2I_{SLP} + K \cdot I_{SLN} \quad (26)$$

Based on (23) and (26), I_{sub} of wide OR gates with CLIL state depends on the fan-in number N and low V_t transistors. Therefore, CLIL state increases I_{sub} as compared to CHIH State. However, due to the stack effect [9] of PDN structure, I_{sub} has weak dependency on N.

V. VERIFICATION AND ANALYSIS

Using physical parameters provided in BSIM4 models, I_{gate} and I_{sub} obtained by proposed models for wide OR domino gates with feature size of 65nm and 45nm are tabulated in Table 1 and also compared with HSPICE simulation results to demonstrate the accuracy of proposed models. As indicated in Table 1, the proposed models are in good agreement with BSIM4 based HSPICE simulation results with errors never exceeding 4%. Therefore, the leakage current with two states can be modeled correctly and the exact optimal sleep state can be obtained to minimize the leakage current of wide domino OR gates. It should be noted that as compared to models of I_{sub}, I_{gate} models yield to a larger over-estimate and under-estimate error because I_{gate} models fail to account for the voltage drop and I_{gate} produced by PMOS transistors, as mentioned in the previous analysis.

Table 1: Comparison of leakage current obtained from model and HSPICE simulation

T (°C)	I_{gate} (nA) CHIH 45nm				I_{gate} (nA) CHIH 65nm			I_{gate} (nA) CLIL 45nm			I_{gate} (nA) CLIL 65nm			I_{sub} (nA) CHIH 45nm			I_{sub} (nA) CHIH 65nm			I_{sub} (nA) CLIL 45nm			I_{sub} (nA) CLIL 65nm		
	N	Est.	Sim	Err %	Est.	Sim	Err %	Est.	Sim.	Err %	Est.	Sim	Err %	Est.	Sim	Err %	Est.	Sim	Err%	Est.	Sim	Err %	Est.	Sim	Err %
25	6	309.5	308.4	0.35	110.0	109.7	0.21	156.5	156.9	0.26	50.91	50.92	0.02	1.426	1.429	0.22	0.97	0.971	0.02	59.12	59.14	0.03	28.28	28.29	0.03
	8	387.1	385.4	0.44	138.3	137.9	0.25	185.5	186.0	0.26	60.43	60.43	0.00	1.426	1.426	0.01	0.97	0.971	0.02	59.25	59.27	0.03	28.32	28.34	0.06
	12	542.3	538.9	0.63	194.9	194.3	0.30	243.7	244.3	0.25	79.47	79.50	0.04	1.426	1.426	0.01	0.97	0.971	0.02	59.41	59.46	0.08	28.38	28.40	0.08
	16	697.5	691.9	0.80	251.6	250.6	0.37	301.9	302.5	0.20	98.50	98.46	0.04	1.426	1.426	0.01	0.97	0.971	0.02	59.52	59.59	0.12	28.41	28.44	0.09
	20	852.7	844.2	1.00	308.2	306.8	0.44	360.1	361.0	0.26	117.5	117.5	0.01	1.426	1.426	0.01	0.97	0.971	0.02	59.59	59.68	0.15	28.44	28.47	0.10
	24	1008	996	1.18	364.8	363.0	0.50	418.3	418.8	0.14	136.6	136.5	0.05	1.426	1.426	0.01	0.97	0.971	0.02	59.65	59.76	0.18	28.46	28.50	0.13
	28	1163	1148	1.34	421.5	419.0	0.58	476.4	476.9	0.09	155.6	155.5	0.08	1.426	1.426	0.01	0.97	0.971	0.02	59.70	59.83	0.23	28.48	28.52	0.14
	32	1318	1298	1.58	478.1	475.0	0.65	534.6	534.9	0.05	174.6	174.6	0.05	1.426	1.426	0.01	0.97	0.971	0.02	59.73	59.89	0.26	28.49	28.54	0.16
	N	Est.	Sim	Err %	Est.	Sim	Err %	Est.	Sim	Err %	Est.	Sim	Err %	Est.	Sim	Err %	Est.	Sim	Err%	Est.	Sim	Err %	Est.	Sim	Err %
110	6	346.0	344.8	0.35	115.0	114.8	0.18	162	168	3.59	51.64	51.81	0.34	60.62	60.69	0.12	6.70	6.70	0.00	1019	1021	0.22	89.66	89.69	0.03
	8	434.0	432.1	0.44	144.8	144.5	0.19	191	198	3.51	61.14	61.41	0.44	60.62	60.68	0.10	6.70	6.70	0.00	1022	1024	0.20	89.86	89.89	0.03
	12	610.1	605.9	0.69	204.3	203.7	0.29	249	258	3.40	80.15	80.43	0.35	60.62	60.68	0.10	6.70	6.70	0.00	1026	1029	0.28	90.13	90.17	0.04
	16	786.2	779.0	0.91	263.8	262.8	0.38	307	319	3.63	99.16	99.54	0.38	60.62	60.68	0.10	6.70	6.70	0.00	1029	1032	0.30	90.31	90.36	0.06
	20	962.3	951.3	1.14	323.3	321.7	0.50	366	379	3.54	118.2	118.6	0.35	60.62	60.68	0.10	6.70	6.70	0.00	1031	1034	0.29	90.44	90.51	0.08
	24	1138	1123	1.32	382.9	380.6	0.59	424	440	3.69	137.2	137.7	0.36	60.62	60.68	0.10	6.70	6.70	0.00	1033	1036	0.32	90.55	90.63	0.09
	28	1314	1293	1.61	442.4	439.3	0.69	482	501	3.80	156.2	156.7	0.31	60.62	60.68	0.10	6.70	6.70	0.00	1034	1037	0.28	90.64	90.73	0.10
	32	1491	1463	1.83	501.9	497.9	0.80	540	561	3.72	175.2	175.8	0.33	60.62	60.68	0.10	6.70	6.70	0.00	1035	1038	0.26	90.71	90.82	0.12

VI. PVT VARIATION AWARE ANALYSIS

Due to the strong dependence of leakage current, it is extremely important to study PVT aware leakage current characteristics of wide OR domino gates, thereby obtaining the optimal sleep state. As mentioned before, the impact of process variation has been evaluated in our previous work [6], which shows that the CLIL state is more robust. This section investigates impact of PVT variation.

A. Impact of temperature variation

Fig. 4 (a) and (b) shows the temperature dependency of leakage current of 65 nm domino OR8 gate. As expected, the impact of temperature variation on I_{sub} is more significant as compared to I_{gate}. As also shown in Fig. 4, the total leakage current with CLIL state is more sensitive to temperature variation compared to CHIH state. This is due to the fact that I_{gate} dominates total leakage current of wide domino OR gates with CHIH state and therefore the total leakage current is relatively insensitive to temperature. Alternatively, as an important contributor, I_{sub} results in larger variations of total leakage current with CLIL state.

B. Impact of voltage supply variation

Fig. 4 (c)-(f) plot the leakage current as a function of supply voltage of 65 nm domino OR8 gate. It can be observed that I_{gate} is more sensitive to supply voltage variation compared to I_{sub}. As shown in Fig. 4, because I_{sub} is a negligible contributor, the variation of total leakage current with CHIH depends on the fluctuation of I_{gate} caused by supply voltage variation. As also can be observed in Fig. 4, at CLIL state, I_{gate} rises quickly with the increasing of supply voltage and catches up with I_{sub} gradually, thereby causing a large spread in total leakage current. Hence, CLIL state is more susceptible to supply voltage variation.

Therefore, the CLIL state is more robust to parameter variation, but it is more susceptible to supply voltage and temperature variations.

C. Impact of PVT variation

To capture the combined effect of PVT variation, most important process parameters including gate length (L_{gate}), channel doping concentration (N_{ch}), and gate oxide thickness (t_{ox}) are assumed to follow Gaussian distribution. And L_{gate}, N_{ch}, and t_{ox} are projected to stay at 3σ =10%, 4%, and 10%, respectively, according to ITRS [6]. Also, voltage supply varies uniformly from $V_{dd}/2$ (0.5V) to V_{dd} (1V) and the range of sleep temperature range of interest is 20-125°C.

1000 Monte Carlo simulations are done and the average leakage current in 65 nm wide domino OR gates under PVT variation are shown in Fig. 5. As shown in Fig. 5, CLIL state is the optimal sleep state to minimize the leakage current for wide domino OR gates at the presence of PVT variation. Also, compared to CHIH state, the effectiveness of CLIL is increased as fan-in number N increases.

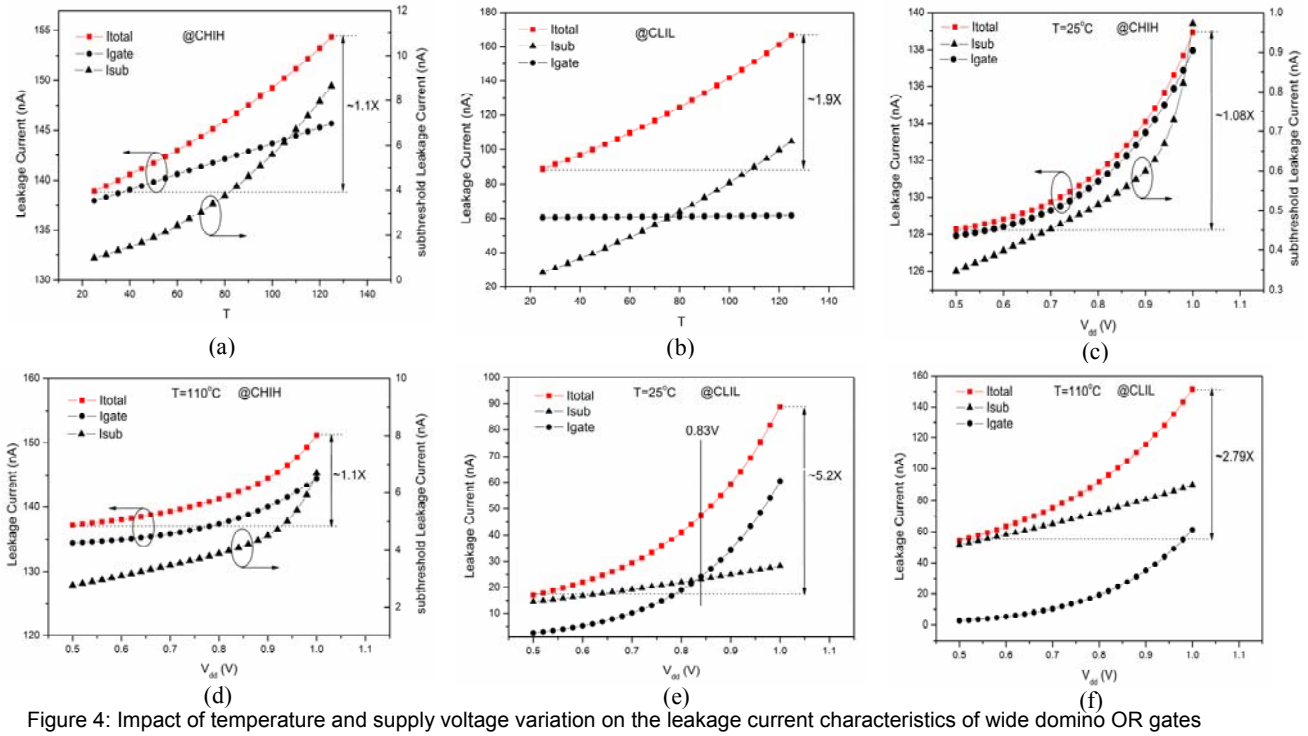


Figure 4: Impact of temperature and supply voltage variation on the leakage current characteristics of wide domino OR gates

VI. CONCLUSION

This paper develops gate-level models for I_{sub} and I_{gate} in wide OR domino circuits with two sleep states and these models can be used to determine the optimal sleep state with minimum leakage current. Results demonstrate that developed models show good agreement with HSPICE simulations. Also, PVT variation aware leakage current characteristics is discussed. It shows that CLIL is the optimal sleep state to achieve low leakage current under PVT variation. It should be pointed out that the developed models in this paper do not depend on specific technology nodes. Also, the methodology for estimating leakage current can be extended to the case of footless domino circuits and other domino logic.

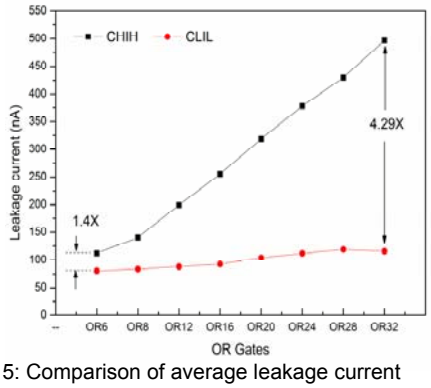


Figure 5: Comparison of average leakage current

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