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Hybrid-cell register files design for improving NBTI reliability

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ABSTRACT

In modern processors, register files (RF) suffers from NBTI induced degradation with technology scaling. In this paper, a hybrid-cell RF design technique is proposed to achieve high reliability by storing the most vulnerable bits in robust 8T cells and other bits in conventional 6T cells. Simulation results in 32 nm predicative CMOS process show that the proposed technique achieves 11.4% and 24.8% RF reliability improvement in high performance system and embedded system, respectively, while the overhead is negligible.

1. Introduction

With the continuous technology scaling, negative Bias Temperature Instability (NBTI) has become one of the major reliability challenges in modern processors. This aging effect is further exacerbated in register files (RF) due to the following two reasons: (1) RF is a hot spot in modern processors and the NBTI effect increases exponentially with temperature; (2) Since RF are accessed very frequently, corrupted data in RF can easily propagate to other parts of microprocessors [1,2]. Recently, Blome et al. [2] observed that, considerable amount of errors affecting a processor usually come from its RF. Therefore, typical high performance systems, such as IBM G5 enterprise server [3], apply some protection mechanisms such as Error Correction Code (ECC). However, the protection scheme comes with significant power and area overheads and it is not applicable for embedded systems under stringent cost constraints.

Consequently, researchers explored many techniques to mitigate NBTI effect in RF. In [4], periodic register rotation was presented to reduce the mismatch between SRAM cell inverter pairs induced by NBTI. However, this technique suffers from large delay penalty due to extra XOR gates in the read/write data paths. In [5], adaptive body biasing technique was employed to reduce the threshold voltage (V_{th}) drift induced by NBTI, but this technique significantly increases the leakage power. In addition, the effect of this technique is reduced with technology scaling. In [6], the empty entries in RF were used to mitigate NBTI stress. However, this technique increases the number of write operations and power consumption.

In this paper, we propose a hybrid-cell RF design to mitigate NBTI induced degradation with low cost. The more vulnerable data bits are stored in the robust 8T cells and the less vulnerable bits are stored in the conventional 6T cells. As a result, the failure probability of RF is significantly decreased, which enables us to enhance the NBTI reliability of RF effectively. Compared to the state of the art, our scheme is different in a couple ways: (1) it offers a simple yet efficient reliable RF design with low cost; (2) it can be applied to improve the NBTI reliability of RF in both high performance systems and embedded processors.

The rest of the paper is organized as follows. In Section 2, the NBTI reliability on SRAM cells is discussed. Section 3 analyzes the bit-aware degradation behavior of RF. Section 4 proposes reliable hybrid-cell RF design. The implementation details and simulation results are provided in Section 5 while Section 6 concludes the paper. Throughout this paper, our experiments are conducted by HSPICE based on 32 nm predictive CMOS process [7].

2. NBTI reliability of SRAM cells

As shown in Fig. 1a, when a pull-up PMOS transistor (P_L or P_R) is negative biased, interface traps are generated at the Si/SiO_2 surface, leading to an increase in the V_{th} of the PMOS transistor. Based on reaction–diffusion (R–D) mechanism [8], V_{th} increase due to the long term NBTI effect can be obtained using the predictive model [7]:

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot T^{0.25} \cdot \left[\frac{1 - \left(1 - \sqrt{\eta(1-\beta)/n}\right)^{2n}}{1 - \left(1 - \sqrt{\eta(1-\beta)/n}\right)^{2}} \right]^{0.5} + \delta_v \qquad (1)$$

where T is the clock period, β the duty cycle, n the number of cycles of stress and recovery, η is 0.35, and K_v is a technology-dependent constant. K_v can be expressed as [7]

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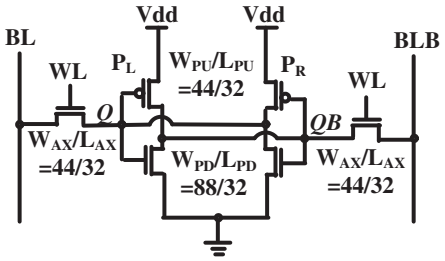
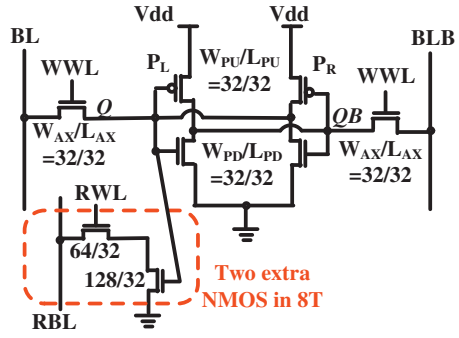
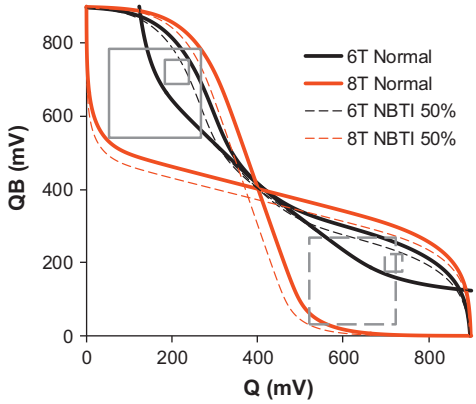


(a) Schematic of 6T SRAM cell



(b) Schematic of 8T SRAM cell



(c) SNM degradation

Fig. 1. Read SNM degradation of SRAM cells with similar performance. (a) The schematic of 6T cell (cell size: 0.24 μm^2); (b) the schematic of 8T cell (cell size: 0.31 μm^2); and (c) comparison of read SNM degradation of two cells due to NBTI.

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}(V_{gs} - V_{th})} \cdot \exp\left(\frac{E_{ox}}{E_0}\right) \cdot \left[1 - \frac{V_{ds}}{\alpha(V_{gs} - V_{th})}\right] \cdot \exp\left(-\frac{E_a}{kT}\right) \quad (2)$$

where k is the Boltzmann constant, C_{ox} the oxide capacitance per unit area, T_{ox} the gate oxide thickness, A, E_0, E_a, α, and δ_v are constants equal to 1.8 mV/nm/C$^{0.5}$, 2.0 MV/cm, 0.13 eV, 1.3, 5.0 mV, respectively.

For the 32 nm technology we use, the initial V_{th} of PMOS devices in SRAM cells is 0.2 V. The supply voltage is 0.9 V and the temperature is 110 °C. Since the V_{th} shift is not sensitive to the duty cycle [9], we neglect the impact of duty cycle in our analysis and assume that it is a constant equal to 0.5. Accordingly, based on the predictive model, we calculate the V_{th} shift due to NBTI effect after seven years, which is the typical lifetime of modern processors [10]. We use the setup approach in [11] to include the calculated V_{th} shift induced by NBTI effect in our simulation.

The NBTI induced V_{th} increase influences the performance of SRAM cells including read stability, write margin, access time, and leakage power. Prior work [12] showed that read stability is the most critical one impacted by NBTI, so we adopted read mode SNM (Static Noise Margin) as the reliability metric in this paper.

Fig. 1 compares the read SNM degradation of SRAM cells induced by NBTI from a graphically viewpoint. In traditional 6T cell (Fig. 1a), transistor strength ratios must be designed carefully to guarantee both successful read and write operations. By adding two NMOS transistors (Fig. 1b), an 8T cell decouples read and write paths, realizing a read-disturb-free operation [13]. Hence, the read SNM of 8T cells is much higher (231 mV) than that of 6T cells (117 mV). More importantly, 8T SRAM cells provide a significant enhancement in NBTI stability as compared to 6T cells, as shown in Fig. 1c. When the zero bias probabilities (ZBP) is 0.5, the read SNM degradation of 8T cells is negligible, while the read SNM of 6T cells degrades by about 15%. However, this good reliability of 8T cells comes with approximately 30% area overhead as compared to conventional 6T cells [13]. Accordingly, if the area is not the first design priority, 8T cells are regarded as the best candidate against NBTI degradation [14,15].

More importantly, since the NBTI effect only happens when the gate of a PMOS transistor is applied by '0', SNM degradation depends on the ZBP of Q strongly. On the one hand, when ZBP is 0.5, the V_{th} shifts of P_L and P_R are balanced, resulting in the best condition with minimum SNM degradation. This is also the basis of many existing techniques such as [4,6], which flipped the stored contents in SRAM cells to achieve the balanced condition. On the other hand, the SNM degradation characteristics of 6T cells are symmetric to the best case (ZBP = 0.5) and the NBTI effect severely increases when ZBP is not 0.5. Especially, in the unbalanced condition with ZBP = 0.99, SNM reduction of 6T cells is nearly 30% [16], which places more emphasis on 8T cells.

3. Bit-aware degradation behavior of RF

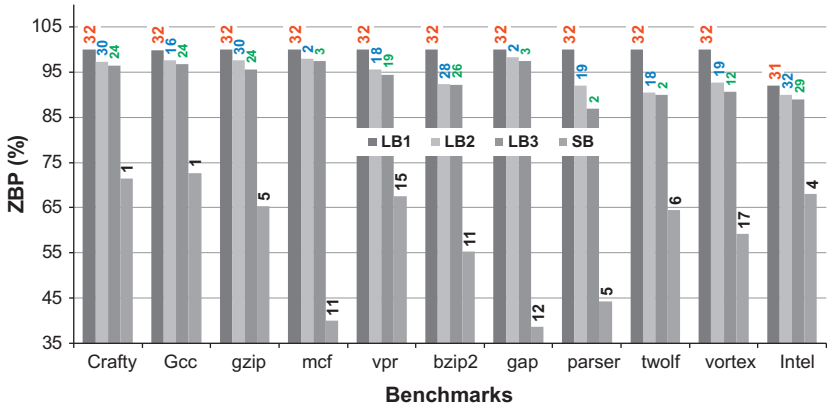
Due to the strong dependency of NBTI effect on ZBP, in this section, we carry out architecture-level simulation to investigate ZBP characteristics of different bits in an integer register and therefore obtain the bit-aware sensitivity to NBTI effect.

To take into account both high performance systems and embedded systems, we selected ten integer benchmarks from SPEC CPU2000 suite and eleven MiBench embedded benchmarks. These benchmarks are compiled for the Alpha ISA and use the reference input set. Based on SimpleScalar simulator [17], we collected RF results from 50,000 Alpha instructions after 20 million fast-forward initialization phase. In addition, our discussion included RF data in [6], which was extracted from 10 million consecutive IA32 instructions based on the Intel® Core™ Microarchitecture.

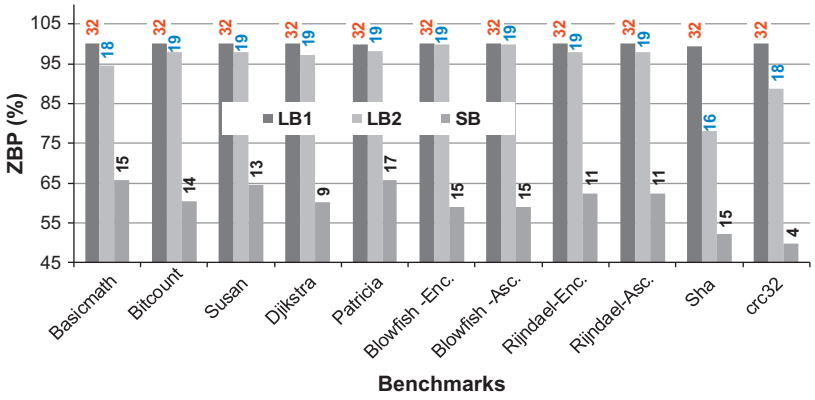
As discussed before, the failure process of RF in two systems are different: with ECC protection, the lifetime of RF in high performance systems is determined by the 3rd failed bit in a register; in embedded systems without ECC, a single bit failure cannot be corrected and the whole register would fail.

Fig. 2 shows the ZBP distribution of 32-bit RF for different applications. We can make the following important observations.

(1) The ZBP of most SB bit (with smallest ZBP value in a register) is larger than 50%, indicating a significant NBTI effect on RF cells.
(2) ZBP of the most significant bit (32 bit) of registers is always close to 100%, which means that this bit is stressed most of the time, leading to higher failure rate as compared to other



(a) RF in high performance systems



(b) RF in embedded systems

Fig. 2. Bit aware degradation behaviors in RF. LB1: the bit with largest ZBP; LB2 (LB3): the bit with second (third) largest ZBP; SB: the bit with smallest ZBP. The numbers shown are the bit positions.

bits. The reason is that most data in registers cannot cover all 32 bits [18]. Therefore, the highest order bit is most sensitive to NBTI effect.

(3) Also, most of registers tend to store more 0's in their higher order bits and store 0s and 1s in lower order bits more randomly, which contribute to the various degradation behaviors of different bits in a register.

4. Proposed robust RF design with hybrid cells

Based on the bit-aware degradation characteristics in RF and reliability of different memory cells, we proposed a hybrid-cell RF design to mitigate the NBTI effect: the higher order bits are stored in robust 8T cells to enhance its reliability and the lower order bits with less sensitivity to NBTI effect are stored in conventional 6T cells to achieve area efficiency.

The schematic of a 32-bit hybrid-cell RF with two reading ports and one writing port (2R1W) is shown in Fig. 3. A 6T cell has only one word line for both reading and writing operations, while an 8T cell has two separate word lines (RWL and WWL) for two operations. In order to achieve effective integration of these two kinds of cells, we adopt the split word line scheme in [19].

The operating principle of the proposed hybrid-cell RF is shown in Fig. 4: in the read operation, write word line (WWL) is disabled and two read word lines RWL1 and RWL2 are enabled to achieve single-ended reading process; during write operation, WWL and RWL1 are both enabled to conduct two access transistors of the 6T bit-cell. This scheme enables zero area overhead of 6T–8T integration [19].

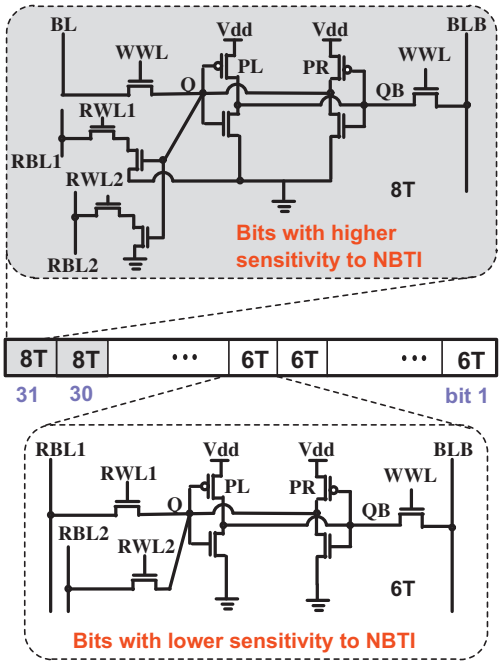


Fig. 3. Schematic and layout design of 32 bit 2R1W hybrid RF.

Note that, in such a 6T–8T hybrid scheme, the half selection problem [13] of 8T cells occurs while writing one bit to RF. We

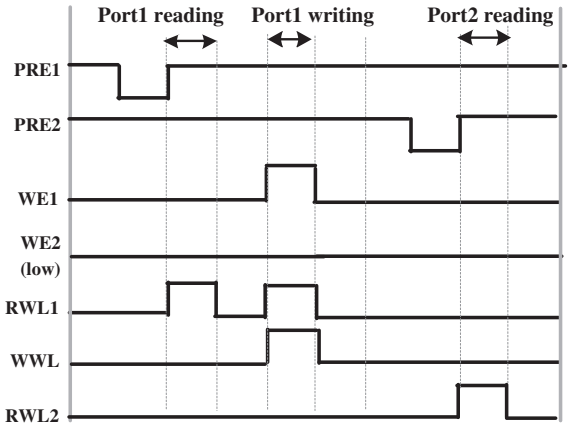


Fig. 4. Timing Diagram for reading and writing operations in proposed RF.

avoided this problem by writing the 32 bits data at the same time. Also, since RF stores more zeros, we placed the two reading ports to the side of *Q*, reducing the large leakage current generated in read bit lines [20].

5. Implementation and experiment result

In order to quantify the reliability improvement after applying our proposed technique, we calculated mean-time-to-failure (MTTF) based on interpolation method in [21]. The failure criterion is SNM < 10% V_{dd}; that is, a cell fails when its read SNM is less than 10% V_{dd}.

A key issue during the implementation of hybrid-cell RF is to select the number of 8T cells in a register.

Based on conservative MOSIS deep sub-micrometer design rules [22], we designed the layout of 6T and 8T cells with 2R1W ports, as shown in Fig. 5. We can see that, compared to a conventional 6T cell, the area of a 8T cell with similar performance is increased from $1512 \times 256\ \text{nm}^2$ to $1268 \times 256\ \text{nm}^2$, resulting in ~19% area overhead. Therefore, we can express the area overhead of a hybrid-cell RF as:

$$\text{Area\_Overhead} \cong \frac{(1+19\%)\times n - n}{N} = \frac{19n}{N}\% \tag{3}$$

where n is the number of 8T cells and N is the total number of cells in a register.

In embedded systems, considering the area constraint, we conservatively choose $n = 1$. So for a 32-bit RF with 2R1W, the area penalty of memory array is only about 0.6%, as shown in Fig. 5a.

In high performance systems, as the number of 8T cells (n) increases, the NBTI reliability would be improved. At the same time, the area overhead becomes larger. Therefore, determining n is an area-reliability optimization problem. Here, we define a new quality metric (HP) for hybrid-cell RF:

$$HP = \frac{\Delta MTTF(n)}{\text{Area\_Overhead}} \tag{4}$$

where the MTTF improvement ($\Delta MTTF(n)$) indicates the NBTI reliability enhancement with n 8T cells as compared to the conventional design with only 6T cells.

Therefore, the optimization problem can now be formulated as

$$n_{opt} = \arg\max_{1\leqslant n\leqslant 32}(HP) = \arg\max_{1\leqslant n\leqslant 32}\left(\frac{\Delta MTTF(n)\cdot N\cdot 100}{19n}\right) \tag{5}$$

For 32-bit RF, N is 32. Accordingly, (5) can be rewritten as

$$n_{opt} = \arg\max_{1\leqslant n\leqslant 32}(HP) = \arg\max_{1\leqslant n\leqslant 32}\left(\Delta MTTF(n)\cdot\frac{169}{n}\right) \tag{6}$$

Based on the Brute–force search algorithm starting with $n = 1$, we can obtain the optimal number of 8T cells (n_{opt}) in a 32-bit register is 4 and the area overhead is 2.2%. Fig. 5b shows the layout design of proposed 32-bit RF in high performance systems.

Fig. 6 shows the MTTF improvement ($\Delta MTTF$) of the proposed RF design. On average, our technique achieves 11.4% and 24.8% RF reliability improvement in high performance system and embedded system, respectively. A key reason is that the existing ECC mechanism in high performance systems reduces the ZBP difference of failed bits, limiting the improvement of hybrid-cell design. Therefore, the proposed technique is especially attractive for embedded systems without expensive protection schemes.

It is important to note that, with the increasing of RF ports, the area overhead in (3) will be reduced. Accordingly, the proposed hybrid-cell technique would provide higher NBTI reliability enhancement with the same implementation cost.

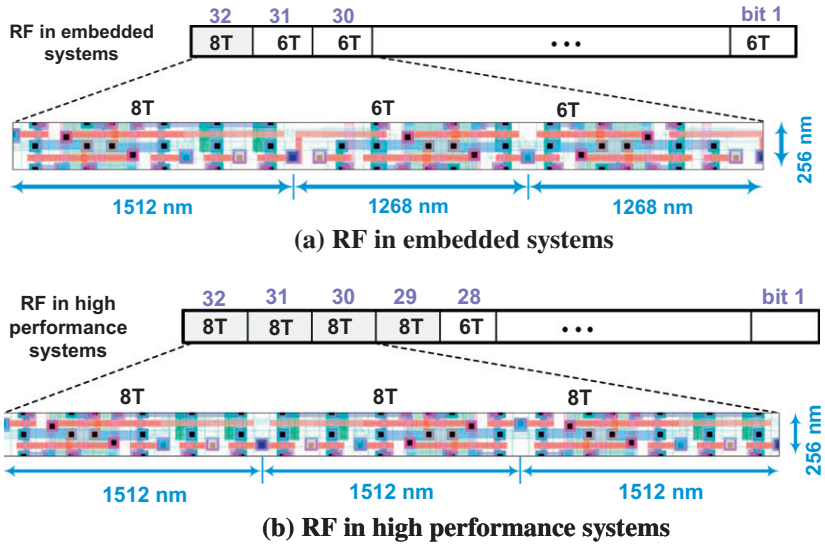


Fig. 5. Layout design of hybrid-cell RF in (a) embedded systems; (b) high perform systems.

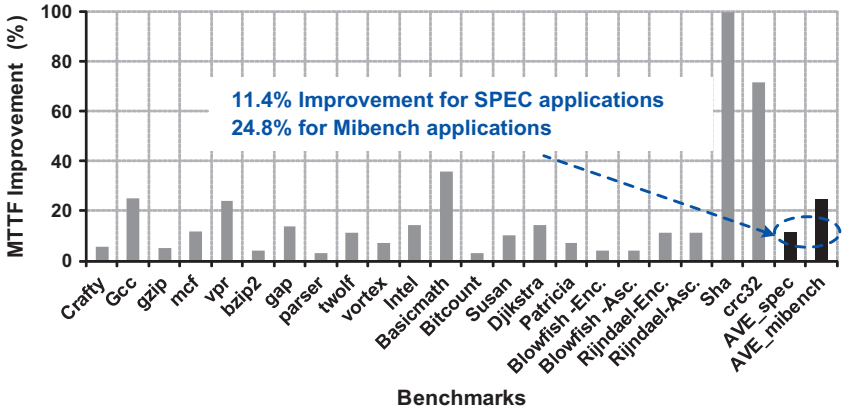


Fig. 6. MTTF improvement.

6. Conclusion

In this paper, we proposed a hybrid-cell RF design to improve NBTI reliability with low cost. The proposed design achieves 11.4% and 24.8% RF reliability improvement with 0.6% and 2.2% area penalty in high performance system and embedded system, respectively. More importantly, the idea presented in this paper can assist NBTI tolerant design of other on-chip memories such as data caches.

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