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Leakage current, active power, and delay analysis of dynamic dual V_t CMOS circuits under P-V-T fluctuations

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ABSTRACT

The leakage current, active power and delay characterizations of the dynamic dual V_t CMOS circuits in the presence of process, voltage, and temperature (P-V-T) fluctuations are analyzed based on multipleparameter Monte Carlo method. It is demonstrated that failing to account for P-V-T fluctuations can result in significant reliability problems and inaccuracy in transistor-level performance estimation. It also indicates that under significant P-V-T fluctuations, dual V_t technique (DVT) is still highly effective to reduce the leakage current and active power for dynamic CMOS circuits, but it induces speed penalty. At last, the robustness of different dynamic CMOS circuits with DVT against the P-V-T fluctuations is discussed in detail.

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1. Introduction

Dynamic CMOS circuits or similar structures are extensively employed in high performance microprocessors and memory [1,2] due to the superior speed and area characteristics. However, along with the progress of advanced VLSI technology, the reduction of the threshold voltage (V_t) and gate oxide thickness (t_{ox}) leads to the exponential increase in the sub-threshold leakage current (I_{sub}) and gate leakage current (I_{gate}), which become a major design challenge. Moreover, in most of current electronic equipments, the clock frequency has been over 1 GHz, which leads to a linear increase in the active power.

The dual V_t technique (DVT) proposed in [3] has been proved to be extremely effective in suppressing I_{sub} of the dynamic CMOS circuits by assigning low V_t devices in the evaluation path and high V_t devices in the pre-charge path, respectively, as shown in Fig. 1. And in the evaluation phase of the dynamic CMOS circuits, the active power contains two parts: dynamic switching power and leakage current power. Therefore, DVT is also an effective technique to decrease the active power.

However, as the technology scales down below 65 nm node, due to the increasing die-to-die and with-in chip fluctuations, new reliability problems are coming into effect. These emerging reliability issues result in device performance degradation and system operation failure. There are three main contributors to fluctuations. They are changes in process parameters, in operating temperatures, and in supply voltage. Process fluctuations occur due to proximity effects in photolithography, non-uniform conditions during deposition and random dopant fluctuation. They result in the fluctuation in V_t which determines the leakage current, active power, and delay of the circuits. Changes in the operating temperature occur because of power dissipation in the form of heat. On-chip thermal fluctuations have a significant bearing on the mobility of electrons and holes, as well as V_t of the devices. And, the leakage current has a linear dependence on the supply voltage swing. Therefore, in nano-scale CMOS technologies, process, voltage, and temperature (P-V-T) fluctuations are crucial reliability concerns. There exists the need to estimate the dynamic CMOS circuit performance under P-V-T fluctuations to help designers judge if the DVT application could meet the reliability related frequency-leakage-power requirements in sub-65 nm era.

Although many researchers have quantified the impact of P-V-Tfluctuations on circuits, there is no known work that has sufficiently described the combined effects of P-V-T fluctuations on leakage current, active power, and delay characteristics. In [4] a full-chip leakage considering uneven voltage drop and uneven temperature is estimated, but it is not a probabilistic approach. In [5] the impact of channel length fluctuations on I_{sub} is studied, but its analysis is based on an empirical relationship between the leakage and the channel length. Moreover, the analysis in [5] cannot be easily extended to P-V-T fluctuations. Although, the work presented in [6–8] develop statistical models to estimate leakage under fluctuations, they fail to account for the combined effects of P-V-T fluctuations. In addition, due to the approximations involved, these analyses are inaccurate as compared to the simulations based on BSIM4 models. Moreover, these models cannot provide the probability distribution function of leakage current. [9-11] have presented leakage characterization under P-V-T fluctuations;





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Fig. 1. Dynamic gates. (a) Low V_t dynamic gate. (b) Dual V_t dynamic gate.

however, none of them take the strong coupling between the leakage and the temperature into consideration. In [12], the impact of P-V-T fluctuations on leakage is accurately modeled, but active power and delay characterizations are not mentioned. The analysis in [13] only refers to dynamic CMOS OR gates, and the process variation model assumes that there is a uniform 10% variation in L_{eff} , N_{ch} , and t_{ox} , which is not reliable enough to account for the process variation.

In this paper, utilizing statistical method – multiple parameter Monte Carlo simulation, the leakage current, active power, and delay characteristics in various dynamic CMOS circuits with DVT is analyzed in the presence of simultaneous *P*–*V*–*T* fluctuations based on the latest ITRS variation model [14].

This paper is organized as follows: in Section 2, the important factors influencing the leakage current, active power and delay characteristics of dynamic circuits is discussed. Section 3 evaluates the effectiveness of DVT under P-V-T variations in detail. Section 4 concludes this work.

2. Dynamic dual V_t CMOS circuits

In this section, the leakage current, active power and delay characteristics of dynamic circuits are discussed analytically.

2.1. Delay time

If we do not consider the delay of the input signal, the delay of dynamic gates can be expressed as [15]

$$t_{\rm delay} = \frac{C_{\rm eval} \cdot V_{\rm dd}}{2I_{\rm DSAT}} = \frac{\left(C_{\rm GD}^{\rm P1} + C_{\rm GD}^{\rm P2} + C_{\rm GD}^{\rm PDN} + C_{\rm G}^{\rm inv} + C_{\rm load}\right) \cdot V_{\rm dd}}{2k_n \cdot (W_{\rm eff}/L_{\rm eff})(V_{\rm GS} - V_t)^{\alpha}}$$
(1)

where C_{eval} is the capacitance of the evaluation node; I_{DSAT} is the saturation current; $C_{\text{GD}}^{\text{P1}}$, $C_{\text{GD}}^{\text{P2}}$, $C_{\text{GD}}^{\text{inv}}$, C_{Ioad} are gate–drain capacitance of the precharger P1, the keeper P2, PDN, the inverter connected to keeper, and loading capacitance (see Fig. 1), respectively; k_n is a technology parameter; α is the velocity saturation exponent ranges from 1 to 2; W_{eff} is the width of the transistors.

from 1 to 2; W_{eff} is the width of the transistors. Noted that, $C_{\text{GD}}^{\text{PDN}}$ is dependent on the fan-in number and PDN structure of a dynamic circuit. In addition, since DVT adopts high V_t transistors, I_{DSAT} is smaller, thereby inducing larger delay time.

2.2. Leakage current

To achieve minimum I_{sub} in the sleep state, the dual V_t dynamic gates are set in CHIH (CLK = 1, In1 = In2 = , . . . , InN = 1) state [3]. Accordingly, the leakage current (I_{leak}) can be expressed as [13,16]

$$I_{\text{leak}} = I_{\text{sub}} + I_{\text{gate}} = \sum_{i} [W_{\text{HN}}]_{i} \cdot J_{\text{SHN}} + \sum_{j} [W_{\text{HP}}]_{j} \cdot J_{\text{SHP}} + W_{\text{LN}} \cdot J_{\text{GFLN}} + \frac{1}{2} \cdot \sum_{i} [W_{\text{HN}}]_{i} \cdot J_{\text{GRHN}} + I_{\text{gate}}^{\text{PDN}}$$

$$(2)$$

where J_{SHN} , J_{SHP} , J_{GFLN} , J_{GRHN} are I_{sub} density per width unit of high V_t NMOS, high V_t PMOS, forward I_{gate} density per width unit of high V_t NMOS, reverse I_{gate} density per width unit of high V_t NMOS, respectively; W_{HN} , W_{HP} , W_{LN} are gate widths of high V_t NMOS, high V_t PMOS, low V_t NMOS (see Fig. 1), respectively; I_{gate}^{PDN} is the I_{gate} generated by PDN, which dominates the total I_{gate} of the dynamic circuit and depends on the fan-in number and PDN structure.

2.3. Active power

The active power is composed of dynamic switching power and leakage current. This subsection focuses on the dynamic switching power. In a dynamic circuit, the dynamic switching power is consumed to charge and discharge the keeper, the evaluation node and the devices in PDN. Accordingly, it can be expressed as [15]:

$$P_{\rm dynamic} = V_{\rm dd}^2 \cdot \left(C_{\rm eval} + C_{\rm GD}^{\rm INV} + C_{\rm G}^{\rm PDN} + C_{\rm G}^{\rm P2} \right)$$
(3)

where C_{GD}^{INV} , C_{G}^{PDN} , C_{G}^{P2} are gate–drain capacitance of the output inverter, the gate capacitance of PDN and the keeper P2, respectively. C_{G}^{PDN} varies with the fan-in number and PDN structure of dynamic circuits.

As given by (1)–(3), the leakage current, active power and delay characteristics of dynamic gates depends on the design parameters (such as fan-in number, size of devices, PDN structure), environmental parameters (such as temperature and supply voltage) and the manufacturing technologies. In the following section, considering these factors, we will present a quantitative analysis to investigate the influence of *P*–*V*–*T* fluctuations on leakage current, active power, and delay characteristics of the dynamic CMOS circuits with DVT.

3. Effectiveness of dual V_t technique under PVT variations

In our analysis, the dynamic circuits with different fan-in numbers and PDN structures, including 2-input, 4-input, 8-input, and 16-input dynamic OR gate (OR2, OR4, OR8, and OR16, respectively), 2-input and 8-input dynamic AND gates (AND2 and AND8), 2-input and 16-input dynamic multiplexer (MUX2 and MUX16), are employed as the benchmark circuits. They are simulated based on 45 nm BSIM4 models by the HSPICE tool [17,18]. The parameters of devices are listed in Table 1. Each dynamic gate drives a capacitive load of 8 fF.

Table 1	
Parameter of devices a	nd P-V-T variations.

Technology node	45 nm BSIM4					
	Low V _t	High V _t				
Device parameters						
NMOS V _t	0.22 V	0.35 V				
PMOS V_t	-0.22 V	-0.35 V				
V _{dd}	0.8 V					
P-V-T variations						
Process (3σ)	Leff	12%				
	t _{ox}	5%				
	V _t	40%				
$V_{\rm dd}$ (3 σ)	10%					
Temperature	110–25 °	C				

The sizing of transistors in different gates is based on two important criteria: all gates are sized to operate at 1 GHZ clock frequency; for the same gates with dual V_t and low V_t techniques, the transistors have the same size, which provides the fair basis of characteristics comparison of two techniques.

Our analysis is based on the *P–V–T* variations specified by latest International Technology Roadmap for Semiconductors (ITRS) [14], which is also listed in Table 1. the process parameters $L_{\rm eff}$, $t_{\rm ox}$, and V_t , and $V_{\rm dd}$ are all assumed to have normal Gaussian statistical distributions with a three sigma (3 σ) fluctuations of 12%, 5%, 40%, and 10%, respectively.

Since temperature variation in practical sleep circuits depends on the interval of sleep mode, and dynamic circuits are typically used in high activity area such as register files, our analysis considers the sleep circuits with short standby intervals and the sleep temperature of circuits will change from the typical working temperature 110 °C to room temperature. Thousand multiple parameter Monte Carlo simulations are done to achieve enough statistical accuracy.

3.1. Leakage current, active power and delay characteristics under PVT variations

In this subsection, the leakage current, active power and delay characteristics of dual V_t dynamic gates are discussed. Fig. 2 shows the distribution curves of 16-input MUX gates with DVT and low V_t techniques as an example. It can be seen that the leakage current distribution curves of two MUX gates cross at 1760 nA. The leakage current of 77% of the samples with DVT is lower than 1760 nA. Alternatively, 57% of the low V_t samples generate leakage current higher than 1760 nA. These results indicate that DVT is highly effective to reduce the total leakage current even under significant P-V-T fluctuations. Also, two active power distribution curves intersect at 22.9 μ W. The active power consumption of 71% of the dual V_t samples is lower than 22.9 μ W and 86% of the low V_t samples consume active power higher than 15 μ W. This is because DVT can be effective to suppress the leakage power, thereby reducing the total active power. As also can be seen from Fig. 2, the delay time of 94% MUX16 sample gates with low V_t technique is smaller than 0.42 ns, while 98% of dual V_t samples is larger than 0.42 ns. Obviously, under the effect of P-V-T fluctuations, the inferior speed characteristics of the high V_t transistors in circuit with DVT still induce the speed penalty, as discussed in Section 2.

Table 2 lists the leakage current, active power, and delay characteristics of OR2, OR4, OR8, OR16, AND2, AND8, MUX2, and MUX16 dynamic gates under P-V-T variations. As indicated, as to leakage power and active power, over 50% samples of all of the dual V_t dynamic gates are smaller than the cross points, and alternatively over 50% samples of all of the low V_t dynamic gates are larger than the cross points. Therefore, under the effect of P-V-T fluctuations,



Leakage Current (nA)

Fig. 2. Leakage current, active power, and delay distribution of 4-input dual V_t dynamic OR gate.

DVT is still quite effective to reduce the total leakage and active power consumption for all style of dynamic gates with speed loss.

3.2. Robustness comparison

This subsection analyzes the robustness (μ/σ – average/standard deviations) of leakage current, active power and delay characteristics of dynamic circuits with DVT. To compare the robustness of two techniques, we also calculate the improvement of robustness with DVT as compared to that with low V_t technique using the following equation:

$$robustness \% = \frac{robust@DVT - robust@low_vt}{robust@low_vt}$$
(4)

where *robust@DVT* and *robust@low_vt* represent the robustness with DVT and low V_t technique, respectively. Obviously, if *robustness* $\% \ge 0$, then DVT improves the robustness of dynamic

Table 2
The average (μ) and standard deviations (σ) of the dynamic gates (leakage: leakage power; active: active power; delay: delay).

Different circuits		Monte Carlo result						Characteristics of distribution curves								
		Leakage (nA)		Active (10^{-5} W)		Delay (10 ⁻¹⁰ s)		Leakage (nA)		Active (10^{-5} W)			Delay (10 ⁻¹⁰ s)			
		μ	σ	μ	σ	μ	σ	Cross	≤ (%)	> (%)	Cross	≼ (%)	> (%)	Cross	≼ (%)	> (%)
OR2	Dual V_t	195	65.8	1.33	0.15	5.99	0.89	247.7	95	5	1.38	70	30	4.72	4	96
	Low V_t	660	574	1.56	0.18	4.25	0.36		26	74		17	83		93	7
OR4	Dual V_t	281	79.4	1.37	0.16	6.15	0.93	324.9	83	17	1.43	71	29	4.73	6	94
	Low V_t	747	584	1.61	0.17	4.19	0.36		21	79		16	84		96	4
OR8	Dual V_t	452	113	1.51	0.19	6.53	0.95	518.4	82	18	1.56	70	30	5.13	4	96
	Low V_t	920	607	1.75	0.19	4.48	0.39		26	74		19	81		95	5
OR16	Dual V_t	872	208	1.90	0.19	5.15	0.85	988	76	24	1.93	61	39	3.69	3	97
	Low V_t	1373	605	2.13	0.20	3.18	0.29		33	67		16	84		97	3
AND2	Dual V_t	560	136	1.81	0.31	6.73	0.90	684.3	87	13	1.82	60	40	5.17	3	97
	Low V_t	1033	626	2.06	0.26	4.45	0.38		37	63		17	83		96	4
AND8	Dual V_t	1852	434	2.03	0.36	7.87	0.87	2084	75	25	2.08	68	32	6.50	4	96
	Low V_t	2382	907	2.33	0.41	5.90	0.38		45	55		33	67		95	5
MUX2	Dual V_t	282	79.6	2.19	0.18	5.44	0.73	324.9	83	27	2.25	71	29	4.54	9	91
	Low V_t	750	560	2.44	0.20	4.11	0.36		20	80		16	84		91	9
MUX16	Dual V_t	1552	370	2.17	0.20	5.61	0.85	1760	77	23	2.29	71	29	4.20	2	98
	Low V_t	2559	803	2.48	0.20	3.65	0.33		43	57		14	86		94	6

circuits; otherwise, adopting DVT will degrade the robustness of circuits.

Table 3 lists the comparison result. We can see that the leakage current robustness of all dual V_t gates are larger than that of the low V_t gates, which shows that DVT can sustain the availability of suppressing leakage current with P-V-T fluctuations. Also observed in Table 3, the delay robustness in all dynamic gates with DVT are lower than that of the low V_t gates. Therefore, while inducing delay penalty, DVT also degrades the immunity of delay characteristics to P-V-T fluctuation.

Another important observation in Table 3 is that, for all circuits with DVT other than OR2, the active power robustness is lower as compared to their low V_t counterparts. But, as discussed in Section

Table 3

The robustness of dynamic gates

3.1, DVT is able to reduce the active power of all gates effectively under P-V-T variations. Therefore, the influence of DVT on overall active power characteristics of dynamic circuits depends on the power reduction, the robustness degradation, and the relative significance of these two factors. Accordingly, to evaluate the overall active power characteristics, we define Improvement-of-DVT (DVT %) as

DVT
$$\% = \lambda \times Power_Reduction\% + (1 - \lambda) \times robustness\%$$
 (5)

where λ is the weighting factor, which indicates the significance of active power reduction and active power robustness in different application cases. Clearly, λ is a real number and $\lambda \in [0, 1]$. In particular, in the extreme case with $\lambda = 1$, the active power reduction is

Circuits	Leakage cu	rrent		Active pow	/er		Delay time			
	Robustness	5	Robustness (%)	Robustness	5	Robustness (%)	Robustness	Robustness (%)		
	Dual V_t	Low V _t		Dual V _t	Low V _t		Dual V _t	Low V _t		
OR2	2.96	1.15	158	8.87	8.67	2.30	6.73	11.81	-43.0	
OR4	3.54	1.28	177	8.56	9.47	-9.59	6.61	11.64	-43.2	
OR8	4.00	1.52	164	7.95	9.21	-13.7	6.87	11.49	-40.2	
OR16	4.19	2.27	85	10.00	10.65	-6.10	6.06	7.48	-44.7	
AND2	4.12	1.65	150	5.84	7.92	-26.3	7.48	11.71	-36.1	
AND8	4.27	2.63	62	5.64	5.68	-0.77	9.05	15.53	-41.7	
MUX2	3.54	1.34	165	12.17	12.5	-0.27	7.45	11.42	-34.7	
MUX16	4.19	3.19	32	10.85	12.4	-12.5	6.60	11.06	-40.3	



Fig. 3. Active power characteristics of dynamic circuits.

the only design concern. *Power_Reduction%* is used to evaluate the active power reduction and it can be expressed as

$$Power_Reduction\% = \frac{power@low_vt - power@DVT}{power@low_vt}$$
(6)

where *power@DVT* and *power@low_vt* represent the active power with DVT and low V_t technique (see Table 2), respectively.

Note that, if DVT% ≥ 0 , the overall active power characteristics of dynamic circuits is improved with DVT under PVT variations.

Fig. 3 shows the DVT% as a function of λ in different gates. We can see that for all circuits, the DVT% increases with the increasing of λ . This is because, the priority of power reduction becomes higher as λ increases, and therefore DVT is more likely to improve the overall active power characteristics. As also can be observed in Fig. 3, the minimum λ value that can achieve improvement of overall active power characteristics (DVT% = 0) is between 0.745 and 0.805, depending on the fan-in number and the PDN structure. For the low fan-in OR gates with DVT (OR2, OR4 and OR8), they show best active power characteristics; for high fan-in OR gates (OR16) and all MUX gates (MUX2 and MUX8) with DVT, they show worst active power characteristics.

4. Conclusion

Due to the increasing die-to-die and with-in chip fluctuations, new reliability problems are coming into effect. These emerging reliability issues result in device performance degradation and system operation failure. In this paper, under significant P-V-T fluctuations, the effectiveness of DVT in dynamic logic design is analyzed based on multiple-parameter Monte Carlo simulation. Our analysis shows that DVT is highly effective to reduce the leakage current and active power consumption in dynamic gates with speed loss. Also, DVT can improve the robustness and heighten the reliability of leakage current in dynamic gates to P-V-T fluctuations. However, DVT degrade the reliability of obtaining constant active power and delay. That is it weakens the immunity of active power and delay characteristics to P-V-T fluctuation. Considering both the active power reduction and robustness degradation, DVT can improve the overall active power characteristics when the relative significance of these two factors is larger than 4.13 (0.805/0.195), therefore DVT has superior reliability to P-V-T fluctuations. The results are a good guide to dynamic logic design with DVT taking reliability issues into account.

In future work, we will tape out enough chips and test them to confirm our simulation results with experiments. Another possible area for future investigation is to design novel dynamic dual V_t circuit to improve the timing yield.

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