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Analysis and optimization of leakage current characteristics in sub-65 nm dual V_t footed domino circuits

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Abstract

The inputs and clock signals combination sleep state dependent leakage current characteristics is analyzed and the optimal sleep state is examined in sub-65 nm dual V_t footed domino circuits. Simulations based on 65 and 45 nm BSIM4 models show that the conventional CHIL state (the clock signal is high and inputs are all low) is ineffective for lowering the leakage current and the conventional CHIH state (the clock signal and inputs are all high) is only effective to suppress the leakage current at high temperature other than the high fan-in domino circuits. For the high fan-in footed domino circuits at high temperature and most of footed domino circuits at room temperature, the CLIL (the clock signal and inputs are all low) state is preferable to reduce the leakage current. Further, the influence of the process variations on the leakage current characteristics of the dual V_t footed domino circuits is also evaluated. It is observed that the average leakage current is universally higher than the date reported in the normal corner and the CLIL state is the optimum choice considering the leakage current reduction and the robustness to the process variations simultaneously.

Keywords: Footed domino circuit; Dual threshold voltage; Leakage current; Process variation

1. Introduction

As a common logic in high-speed performance chip design, domino circuits (dominos) can be classified into footed dominos and footless dominos [1–3]. The footed dominos have better timing characteristics because the footer isolates the pull-down network (PDN) from ground to prevent the PDN altering the state of the dynamic node in the precharge phase. By omitting the footer, the footless dominos reduce both the circuit evaluation delay and the power consumption. In despite of their different characteristics, the footed and footless dominos are both extensively applied in high performance microprocessors. In a multi-stage dominos, the first stage is typically footed and the other are footless ones [3].

However, both footed and footless dominos are less power effective compared to the static logic. Especially with aggressive device scaling, the threshold voltage (V_t) scaling accompanies with the exponential increase in the sub-threshold leakage current (I_{sub}), which is a concern for not only power consumption but also noise immunity.

To tackle the high I_{sub} problem, many circuit level approaches have been proposed including transistors stack effect [4], body-bias control [5], input vector control [6], dual V_t CMOS [7], and so on. The dual V_t CMOS technique proposed in Ref. [7] is shown to be especially efficient for dominos due to this circuit logic has the fixed transition directions. The dual V_t footless domino technique [7] is realized by assigning low V_t devices in the evaluation path while high V_t devices are used in the precharge path of the circuits.

Kao et al. in Ref. [7] indicated that a high clock signal with high inputs (CHIH) is preferable to reduce I_{sub} of a sleep dual V_t footless domino gate. Based on Kao's found, previous works in the area of footed dominos also adopt the CHIH state to reduce the leakage current of sleep circuits. These include the NMOS-sleep dominos [8], the sleep dominos [9], the low swing low power dominos [10], and so on.

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However, the CHIH sleep state produces great gate leakage current (I_{gate}) through the PDN transistors in both footed and footless dominos. In fact, I_{gate} increases exponentially with the scaling of the oxide thickness (t_{ox}). 2003 International Technology Roadmap for Semiconductors (ITRS) predicts that oxide thickness will decrease from 13 Å for the 65 nm generation to 9 Å for 35 nm [11]. With such thin t_{ox}, accordingly, I_{gate} is becoming a significant contributor to the total leakage current as CMOS process advances to sub-65 nm regime.

More recently, comprehensive analysis of the total leakage including I_{sub} and I_{gate} of footless dominos was carried out by Liu and Kursun [12]. Considering the impact of I_{gate} on the total leakage current, the study indicates that a high clock signal with low inputs sleep state (CHIL) is preferable in dual V_t footless dominos, particularly at low sleep temperatures.

However, for footed dominos with CHIL sleep state, the PDN exhibits great I_{sub} and the footer is in the maximum I_{gate} state. Thus, the CHIL sleep state does not solve the leakage current problem completely.

In this paper, we study the sources of leakage current in dual V_t footed dominos and show that I_{sub} and I_{gate} are actually a function of not only inputs state but also the clock signal state. From the observation of the combined optimization problem, a quantitative study of the influence of inputs and clock signal combination states on the leakage current of the sleep dual V_t footed dominos is provided to optimize the total leakage current. Also, considering the influence of process parameter variations on the leakage current, different sleep states are compared to minimize the total leakage current. In addition, the robustness of dual V_t footed dominos with different sleep states to the process parameter variations is studied.

The remainder of the paper is organized as follows. In the next section, the leakage current conduction in dual V_t footed dominos is analyzed. In Section 3, simulation results characterizing the leakage current of the dual V_t footed dominos are presented and discussed. The leakage current characteristics of dual V_t footed dominos under the influence of the process parameter variations is investigated in Section 4. Finally, the conclusions are offered in Section 5.

2. Leakage current analysis in dual V_t footed dominos

In this section, the leakage current conduction is analyzed firstly in the dual V_t footed dominos with different sleep state in detail. And in the second part the I_{sub} and I_{gate} analysis of a single transistor is presented.

2.1. Leakage current conduction in the dual V_t footed dominos

The leakage current conduction paths in the dual V_t footed dominos with different sleep states are identified. To make this discussion more clear, consider a typical two-input dual V_t footed domino AND gate with the conventional CHIH and CHIL states as shown in Fig. 1. It can be seen that there are multiple sources of I_{gate} in a dual V_t footed domino circuit, but this work aims to reduce I_{gate} through the PDN and the footer (PDNF). One reason for this is that the remaindings of dominos are PMOS and high V_t NMOS transistors, which all produce less I_{gate} than the low V_t NMOS transistors in the PDNF. Second, the remaindings of different logic dual V_t footed dominos have the same structure, and yet the number of the PDNF is increased with the increasing of the fan-in. Thus, I_{gate} through the PDNF plays a crucial role in determining the total I_{gate}, especially in the high fan-in dominos.

Since the PDNF consists of low V_t NMOS transistors, I_{gate} of a single low V_t NMOS transistor is analyzed before the detailed analysis of the leakage current of the dual V_t footed dominos.

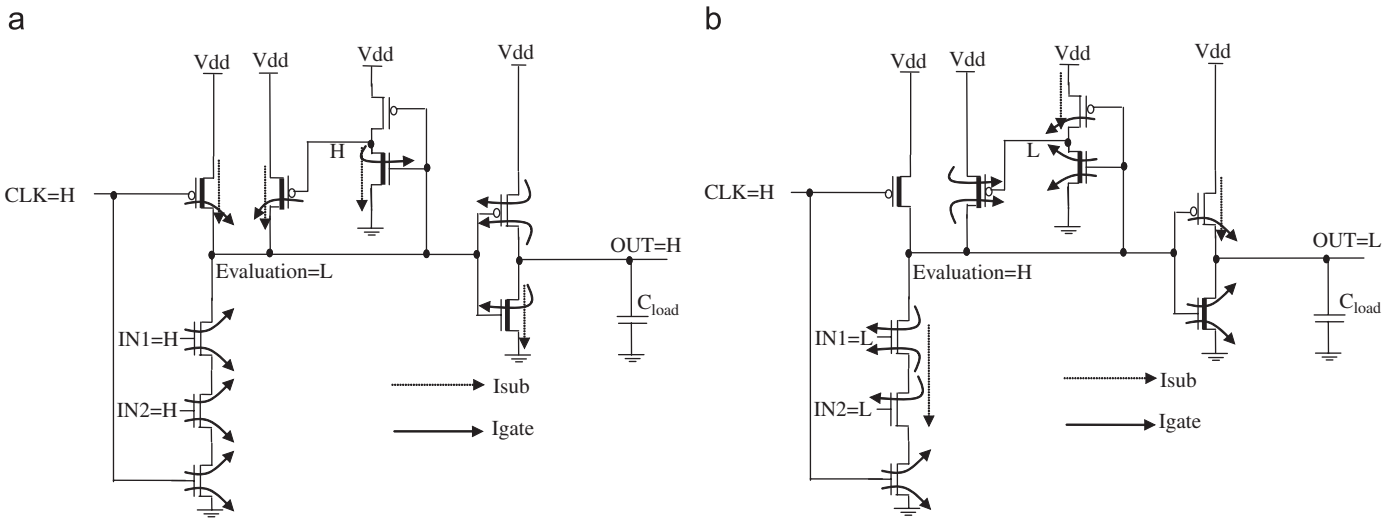

Fig. 1. Variation of the I_{sub} and I_{gate} conduction paths with the two conventional sleep states in a two-input dual V_t footed domino AND gate: (a) CHIH and (b) CHIL. The high V_t transistors are symbolically represented by a thick line in the channel region.

2.1.1. I_{gate} analysis of a low V_t NMOS transistor

Fig. 2 shows the four possible biasing states for a low V_t NMOS transistor in the PDNF in footed dominos [13]. S1 is in the zero biasing and S2 is in the edge reverse biasing. Also, S3 and S4 represent the reverse and forward biasing, respectively.

Table 1 lists I_{gate} for a low V_t NMOS at four different possible bias conditions with technology scaling at the two typical temperatures. It is confirmed that I_{gate} of NMOS in 45 nm technology is bigger than that in 65 nm technology at the same biasing conditions. Simulation results also confirm that I_{gate} is weakly dependent on the temperature [14]. Most importantly, the zero biasing state 1 does not produce I_{gate}. The state 4 produces the greatest forward I_{gate}, and state 3 exhibits smaller reverse I_{gate} compared to the forward I_{gate}. The edge reverse I_{gate} at state 2 is further smaller than the forward and reverse ones.

2.1.2. Leakage current analysis in dual V_t footed dominos with different sleep state

As illustrated in Fig. 1, when the footed dominos are in the conventional CHIH and CHIL states, its leakage current characteristics is similar to the footless conditions analyzed in Ref. [12]. The CHIH state turns off all of the high V_t transistors, suppressing I_{sub}. But the PDNF are all turned on with high V_{gs} and V_{gd} and hence in S4, which leads to the greatest forward I_{gate}. To reduce I_{gate}, the CHIL state cuts off the NMOS transistors in the PDN, which produce reverse and edge reverse I_{gate}. But in this case, significant I_{sub} flows through the PDN. Further, in the CHIL state, the footer exhibits maximum forward I_{gate} due to the high clock signal, which imposes a serious limitation to the leakage current reduction that can be provided by the dual V_t technique.

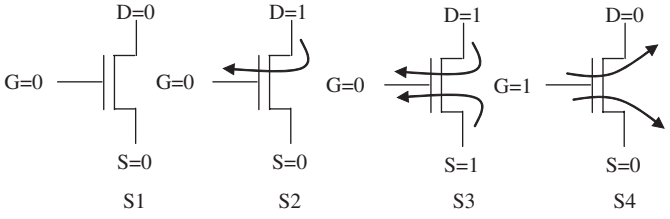

Fig. 2. Four possible biasing states for a low V_t NMOS transistor in the PDNF in footed dominos.

Table 1
I_{gate} for a low V_t NMOS at four different possible bias conditions with technology scaling at the two typical sleep temperatures

Technology (nm)	T (°C)	I_{gate} (nA)			
		S1	S2	S3	S4
65	110	0	2.768	55.36	86.67
	25	0	2.768	55.36	82.38
45	110	0	84.72	169.4	256.3
	25	0	84.72	169.4	226.0

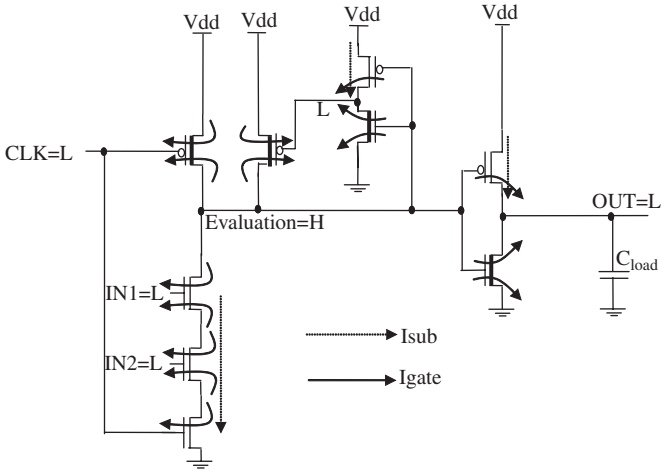

Fig. 3. Variation of the I_{sub} and I_{gate} conduction paths with CLIL state in a two-input dual V_t footed domino AND gate.

Therefore, if the clock signal is set low, I_{gate} will be considerably depressed compared to the conventional two states. And for footed dominos, no matter the clock signal is high or low, one of the pull-up and footer transistors is turned off, ensuring that no short-circuit current conduction between the power supply and grand. So it is reasonable to set the clock signal low. When the clock signal is low, there are two states with the high inputs (CLIH) and low inputs (CLIL), respectively. Due to the low clock signal, the CLIL and CLIH states both produce low output. Since in a domino chain, the output of a domino gate will drive other similar domino gates. Accordingly, the CLIH state is impractical in the domino chains.

Thus, to suppress the leakage current effectively, the CLIL sleep state need to be considered as shown in Fig. 3. For the CLIL state, since all the transistors in the PDNF are turned off, reverse and edge reverse I_{gate} exist in the PDNF, which is smaller than those in the CHIH and CHIL states. Also, the off PDNF in series prevents I_{sub} from increasing greatly due to the stack effect [4]. Hence, the CLIL state suppresses I_{gate} greatly and produces middling I_{sub}, compared to the CHIH and CHIL states.

Notice that, in general, the CHIH minimizes I_{sub}, the CLIL state leads to minimum I_{gate}, and the CHIL state has little its own predominance compared to the others. And between CHIH and CLIL states, which one is better for the total leakage current minimization is dependent on the relative contribution of I_{sub} and I_{gate} to the total leakage current. If I_{gate} is the highest source, the CLIL state is preferable. Alternatively, if I_{sub} dominates the leakage current, the CHIH state is the best choice.

2.2. I_{sub} and I_{gate} analysis of a single transistor

In this part, the comparison of I_{sub} and I_{gate} of a single transistor is analyzed and the results are shown in Fig. 4. It is can be seen that I_{sub} produced by the low V_t transistors is

the highest source of leakage current in sub-65 nm technologies at 110 °C. It is important to note that, for the 65 nm technology at 110 °C, the gap between I_{gate} and I_{sub} of the low V_t transistors is much narrower than that in the 45 nm technology.

At 25 °C, I_{gate} produced by low V_t NMOS transistors in the PDNF is the dominant source of the leakage current in sub-65 nm technologies, as shown in Fig. 4.

The opposite results at two typical sleep temperatures are due to the different dependence of I_{sub} and I_{gate} on the temperature [14]. At low temperature, I_{gate} is the bigger contributor and it has a very weak dependence on temperature. And yet I_{sub} increases exponentially with the temperature increasing, therefore, it dominates the leakage current at high temperature. However, for a domino circuit composed of many transistors, the relative contribution of I_{sub} and I_{gate} also varies with the fan-in, structure of the PDN [12]. It is shown that a quantitative analysis is needed to identify the optimum combination state of the inputs and clock signal with the minimum total leakage current at two typical sleep temperatures in sub-65 nm era.

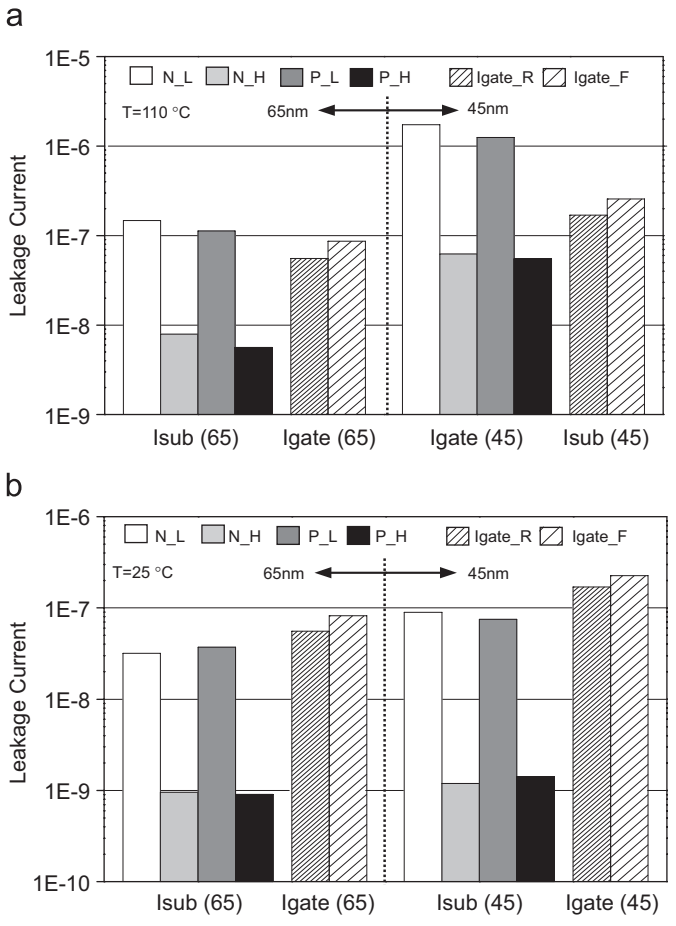

Fig. 4. Comparison of I_{sub} and I_{gate} of a single sub-65 nm transistor at two typical sleep temperatures: (a) 110 °C and (b) 25 °C (N_L, low V_t NMOS; N_H, high V_t NMOS; P_L, low V_t PMOS; P_H, high V_t PMOS; I_{gate}_R, reverse I_{gate}; and I_{gate}_F, forward I_{gate}).

3. Leakage current characteristics of dual V_t footed dominos with different sleep states

In the following experiments, the leakage current characteristics of sleep dual V_t footed dominos with different fan-in and PDN structure at two typical sleep temperatures is evaluated for CMOS 65 and 45 nm BSIM4 models [15], respectively. All the parameters are listed in Table 2. The benchmark circuits are all sized to operate with a 1 GHZ clock at a worst case temperature of 110 °C. To have a comparison, the transistors in each type dominos have the same physical size, respectively.

3.1. Leakage current at high temperature

In this part, it is assumed that the sleep mode is short and the temperature keeps 110 °C during the short sleep period. The leakage current of dual V_t footed dominos with three states is shown in Fig. 5. As discussed above, I_{sub} produced by the low V_t transistors is the highest source of leakage current in sub-65 nm technologies at 110 °C. The CHIH state is, therefore, preferable to suppressing the total leakage current in the majority of dual V_t footed dominos except a 16-bit multiplexer (MUX16), as shown in Fig. 5. However, as the increasing of parallel PDN paths, I_{gate} rises and catches up with I_{sub} gradually. Thus, I_{gate} becomes the bigger contributor in high fan-in wide dominos. For the MUX16 gate, therefore, the CLIL state minimizes the leakage current. Simulation results show a leakage improvement of upto 72% and 42% as compared to the CHIH state in 65 and 45 nm technology, respectively. Since for the 65 nm technology the gap is much less than the 45 nm technology, as mentioned before, I_{gate} is able to catch up with I_{sub} faster, therefore, the effectiveness of the CLIL state decreases with the technology scaling, as indicated in Fig. 5.

3.2. Leakage current at low temperature

In this part, it is assumed that the sleep period is long and the sleep temperature has fallen to the room temperature.

The leakage current of dual V_t sleep footed dominos with three sleep states at 25 °C is shown in Fig. 6. At 25 °C, I_{gate} produced by the low V_t NMOS transistors in the PDNF is the dominant source of the leakage current in sub-65 nm technologies (Fig. 4). Thus, unlike the previously published

Table 2
Process parameter

Parameter	65 nm	45 nm
V_{DD}	1 V	0.8 V
L_{eff}	65 nm	45 nm
V_t of high V_t devices	0.35 V/−0.35 V	0.35 V/−0.35 V
V_t of low V_t devices	0.22 V/−0.22 V	0.22 V/−0.22 V
HSPICE LEVEL	54	54

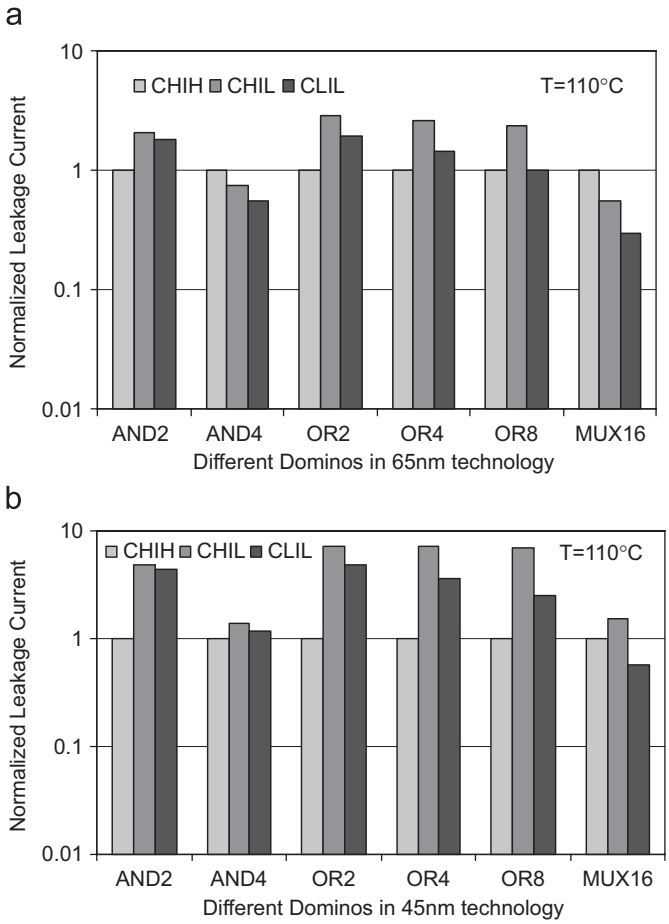

Fig. 5. Comparison of the total leakage current of dual V_t footed dominos with three sleep states at 110 °C. The leakage currents are all normalized to the total leakage current of corresponding gates with the CHIH state.

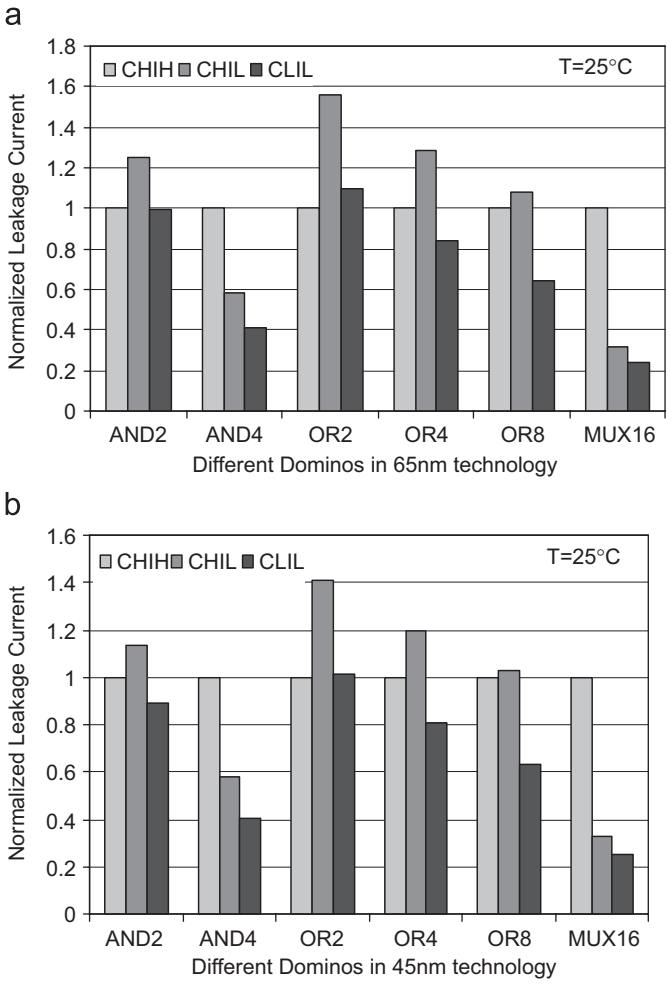

Fig. 6. Comparison of the total leakage current of dual V_t footed dominos with three sleep states at 25 °C. The leakage currents are all normalized to the total leakage current of corresponding gates with the CHIH state.

results, the CLIL state is preferable for minimizing the total leakage current in most dual V_t footed dominos except the OR2 gate (Table 3). And the effectiveness of the CLIL state will become enhancive with the increasing of the fan-in, reducing the total leakage current by up to 76% and 75% in 65 and 45 nm technology respectively, when compared to the conventional CHIH state.

4. Process parameter variations

As the CMOS process advances to sub-65 nm era, scaling has resulted in significant increase in the variations of the process and design parameters, including the most important parameters gate length (L_{gate}), channel doping concentration (N_{ch}), and t_{ox} [16–19]. Hence the process variations have a significant effect on the leakage current due to its strong dependence on the parameters. To evaluate the impact of process variations in L_{gate}, N_{ch}, and t_{ox} on the leakage current of the dual V_t footed dominos with different sleep state, 1000 Monte Carlo simulations are done in 65 nm CMOS technology. In the simulation, each parameter is assumed to follow a Gaussian statistical distributions, with a three sigma (3σ) variation of 10% [12].

Table 3
Total leakage current of dual V_t dominos in 65 nm CMOS technology at two typical sleep temperatures

T (°C)	State	Total leakage current (μA)					
		AND2	AND4	OR2	OR4	OR8	MUX16
110	CHIH	0.361	2.059	0.062	0.092	0.151	8.824
	CHIL	0.747	1.514	0.177	0.234	0.356	4.883
	CLIL	0.643	1.150	0.121	0.132	0.151	2.596
25	CHIH	0.315	1.899	0.054	0.082	0.139	8.353
	CHIL	0.395	1.105	0.085	0.106	0.151	2.649
	CLIL	0.312	0.775	0.059	0.069	0.088	1.980

Fig. 7 shows the leakage current distribution curves of the MUX16 with three different sleep states at two typical sleep temperatures as an example. It can be seen that the distribution curves of the CHIH and CLIL states cross at 1.49 and 1.12 μA at high and low temperatures, respectively. At 110 °C, 85% of the samples with the CLIL state produce leakage current lower than 1.49 μA and the leakage current of 75% of the samples with the CHIH state is higher

than 1.49 μA. Alternatively, 91% of the samples with the CLIL state produce leakage current lower than 1.12 μA and the leakage current of 83% of the samples with the CHIH state is higher than 1.12 μA. These results indicates that the CLIL state are preferable to reduce the total leakage current in majority of the samples under process parameter fluctuations at both high and low temperatures, which is similar to the analysis of the normal one.

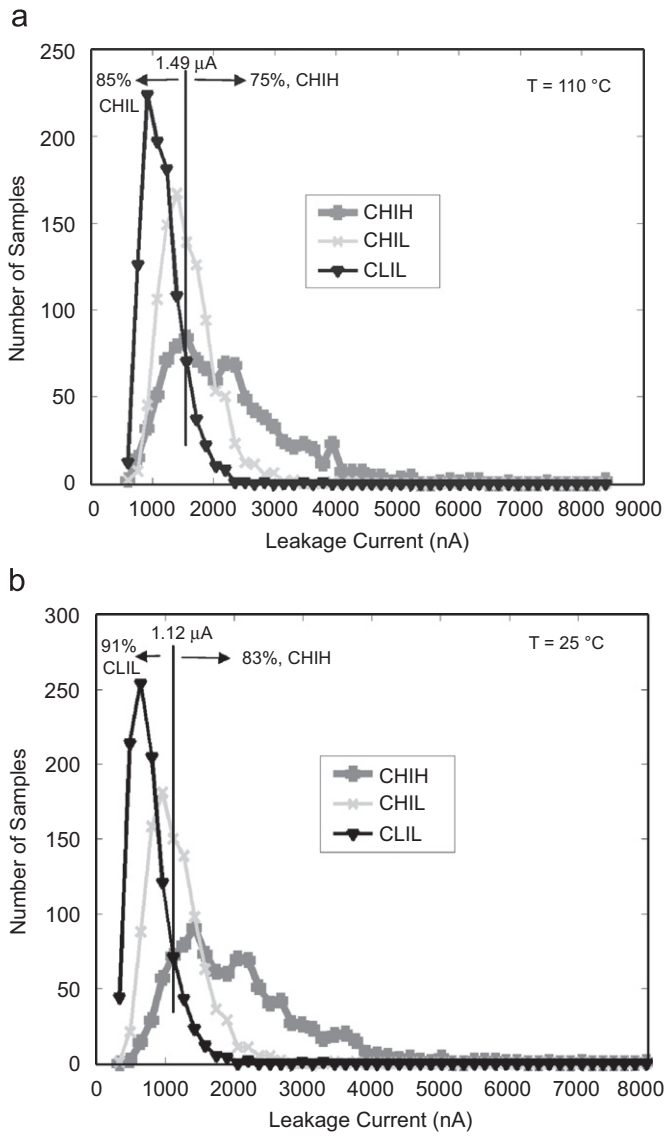

Fig. 7. Distribution of leakage current of MUX16 gate at two typical sleep temperatures: (a) 110 °C and (b) 25 °C.

As listed in Table 4, the average leakage current obtained by Monte Carlo simulation is universally higher than the date reported in the normal corner (Table 3), whereas the comparison of the three sleep states is in a like manner.

To better investigate the impact of the process variation on the leakage current variations of dual V_t footed dominos, we compare the parameter uncertainty (U) of dominos in different sleep states. Here U is given as the standard deviation (S.D.) of leakage divided by its average value, which is similar to the definition in Ref. [18].

As implied by the results from Table 5, the CHIH state is highly susceptible to the manufacturing variations compared to the other two states. Between the CHIL and CLIL states, the former is more robust to process variations in AND type dual V_t footed dominos and the latter improves the robustness of OR type dual V_t footed dominos. This implies that, the CHIH state and the CLIL state are more effective to reduce the leakage current alone. And the CLIL state can optimize the current considering the process variations.

5. Conclusions

This paper embarks on a comprehensive quantitative approach to leakage current characteristics analysis and optimization in sub-65 nm dual V_t footed dominos. To the best of our knowledge, for the first time, the dependence of the sub-threshold leakage and gate leakage current upon the combination of the inputs and the clock signal states is presented. It is shown that in the sub-65 nm technology domain, with the increasing contribution of gate leakage current towards the total leakage current, the conventional CHIH and CHIL states are not adequate sleep setup for dual V_t footed dominos. Hence the CLIL state is advanced and the inputs and clock signals combination sleep state dependent total leakage current characteristics is examined and optimized.

Simulations based on 65 and 45 nm BSIM4 models have been performed. It is observed that the conventional CHIL state is ineffective for lowering the leakage current and the CHIH state is only effective to suppress the leakage current

Table 4
Average and standard deviation of leakage current of dual V_t dominos in 65 nm CMOS technology at two typical sleep temperatures

T (°C)	State	Average and standard deviation (Average/SD) of total leakage current (μA)					
		AND2	AND4	OR2	OR4	OR8	MUX16
110	CHIH	0.401/0.156	2.297/1.027	0.069/0.027	0.102/0.044	0.169/0.078	9.854/4.928
	CHIL	0.790/0.154	1.646/0.437	0.187/0.036	0.250/0.051	0.374/0.086	5.248/1.550
	CLIL	0.676/0.136	1.237/0.336	0.127/0.024	0.139/0.027	0.161/0.034	2.826/0.866
25	CHIH	0.353/0.149	2.126/0.982	0.061/0.025	0.092/0.042	0.156/0.075	9.351/4.747
	CHIL	0.432/0.110	1.227/0.401	0.092/0.023	0.116/0.032	0.164/0.050	2.934/1.113
	CLIL	0.338/0.089	0.854/0.307	0.065/0.016	0.075/0.019	0.097/0.027	2.195/0.820

Table 5
Leakage uncertainty (U) of dual V_t footed dominos in 65 nm CMOS technology at two typical sleep temperatures

T (°C)	State	Leakage uncertainty (U)					
		AND2	AND4	OR2	OR4	OR8	MUX16
110	CH IH	0.389	0.447	0.388	0.428	0.463	0.500
	CH IL	0.156	0.266	0.191	0.205	0.229	0.295
	CL IL	0.201	0.271	0.192	0.192	0.209	0.306
25	CH IH	0.421	0.462	0.421	0.453	0.480	0.507
	CH IL	0.256	0.327	0.256	0.274	0.304	0.379
	CL IL	0.265	0.359	0.251	0.252	0.280	0.373

at high temperature other than the high fan-in dominos. Another observation is that the CLIL state reduces the leakage current in high fan-in wide dominos and most of dominos at room temperature by up to 76% depending on technology and circuit structure, compared to the CHIH state. Finally, the leakage current characteristics of the dual V_t footed dominos under the influence of process parameter variations is assessed. It shows that the average leakage current is universally higher and the comparison of the three sleep states is in a like manner compared to that in the normal corner. Our study further shows that the CHIH state is the most sensitive to the process parameter variations and the CLIL state is the optimal choice considering both robustness and leakage current reduction simultaneously.

References

[1] H. Mahmoodi-Meimand, K. Roy, A leakage-tolerant high fan-in dynamic circuit design style, in: Proceedings of IEEE International Systems-On-Chip Conference (2003) 117–120.

[2] J.-S. Wang, S.-J. Shieh, C. Yeh, Y.-h. Yeh, Pseudo-footless CMOS domino logic circuits for high-performance VLSI designs, Proc. ISCAS (2004) 401–404.

[3] V. Kursun, E.G. Friedman, Domino logic with variable threshold voltage keeper, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 11 (6) (2003) 1080–1093.

[4] S. Heo, K. Asanović, Leakage-biased domino circuits for dynamic fine-grain leakage reduction, in: 2002 Symposium on VLSl Circuits Digest (2002) 316–319.

[5] A. Keshavarzi, S. Narendra, S. Borkar, C.F. Hawkins, K. Roy, V. De, Technology scaling behavior of optimum reverse body bias for standby leakage power reduction in CMOS IC's, Int. Sympos. Low Power Electron. Design (1999) 252–254.

[6] A. Abdollahi, F. Fallah, M. Pedram, Leakage current reduction in CMOS VLSI circuits by input vector control, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 12 (2) (2004) 140–153.

[7] J.T. Kao, A.P. Chandrakasan, Dual-threshold voltage techniques for low power digital circuits, IEEE J. Solid-State Circuits 35 (7) (2000) 1009–1018.

[8] G. Yang, Z. Wang, S. Kang, Leakage-proof domino circuit design for deep sub-100 nm technologies, Proc. IEEE Int. Conf. VLSI Design (2004) 222–227.

[9] V. Kursun, E.G. Friedman, Sleep switch dual threshold voltage domino logic with reduced standby leakage current, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 12 (5) (2004) 485–496.

[10] Guo Baozeng, Gong Na, Wang Jinhui, Leakage-proof and high performance domino circuit design for sub-70 nm CMOS technologies, Chin. J. Semicond. 27 (5) (2006) 159–166.

[11] International Technology Roadmap for Semiconductors, 2003 ⟨http://public.itrs.net/⟩.

[12] Z. Liu, V. Kursun, Leakage power characteristics of dynamic circuits in nanometer CMOS technologies, IEEE Trans. Circuits Syst. II 53 (8) (2006) 692–696.

[13] H. Rahman, C. Chakrabarti, A leakage estimation and reduction technique for scaled CMOS logic circuits considering gate-leakage, IEEE Int. Sympos. Circuits Syst. (2004) 297–300.

[14] A. Vladimirescu, C. Yu, O. Thomas, Q. Huifang, D. Markovic, A. Valentian, R. Ionita, J. Rabaey, A. Amara, Ultra-low-voltage robust design issues in deep-submicron CMOS, in: The 2nd Annual IEEE Northeast Workshop (2004) 49–52.

[15] Predictive Technology Model (PTM), ⟨http://www.eas.asu.edu/~ptm⟩.

[16] K. Meng, R. Joseph, Process variation aware cache leakage management, Proc. ISLPED (2006) 262–267.

[17] S. Bhardwaj, Y. Cao, S. Vrudhula, Statistical leakage minimization through joint selection of gate sizes, gate lengths and threshold voltage, in: Proceedings of the 2006 Conference on Asia South Pacific Design Automation (2006) 953–958.

[18] Y.-F. Tsai, N. Vijaykrishnan, Y. Xie, M.J. Irwin, Influence of leakage reduction techniques on delay/leakage uncertainty, Proc. VLSI Design (2005) 374–379.

[19] A.N. Chandorkar, Ch. Ragunandan, P. Agashe, D. Sharma, H. Iwai, Impact of process variations on leakage power in CMOS circuits in Nano era, Proc. ICSICT (2006) 1248–1251.