Dual-Rail Combinational Circuit Design Example Problems

1) Design a fully observable and input-complete dual-rail 2:1 multiplexer **having a worse-case delay of no more than two gates**. The inputs are $D0$, $D1$, and $S$, and the output is $F$, all of which are dual-rail signals.

2) Design a maximum speed, minimal area circuit for an unsigned 2-bit dual-rail NCL adder: $S(2:0) = A(1:0) + B(1:0)$. **Do not use half-adders and full-adders.** The circuit must be input-complete and observable. Hint: the worse case delay is 2 gate delays.